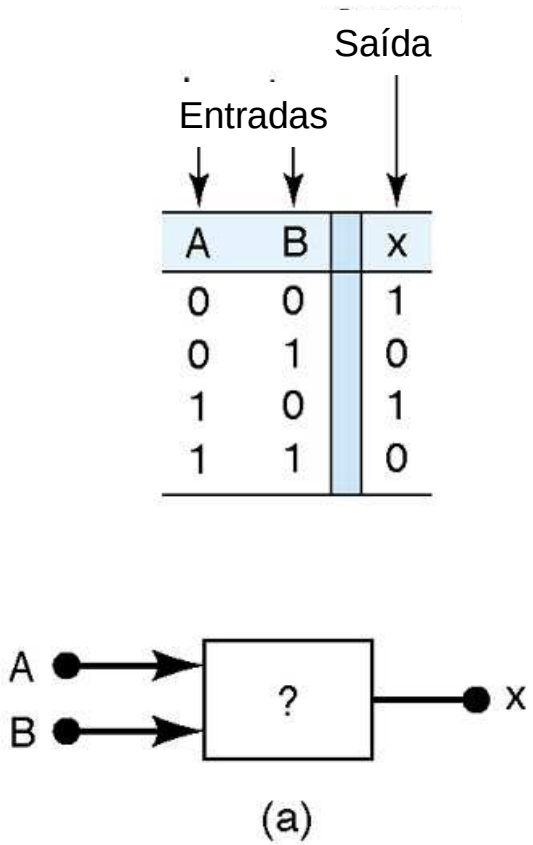
FIGURA 3-1 Exemplos de tabelas –verdade para circuitos de: (a) duas entradas, (b) três entradas e (c) quatro entradas.



(a)

A	B	C	x
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

(b)

A	B	C	D	x
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

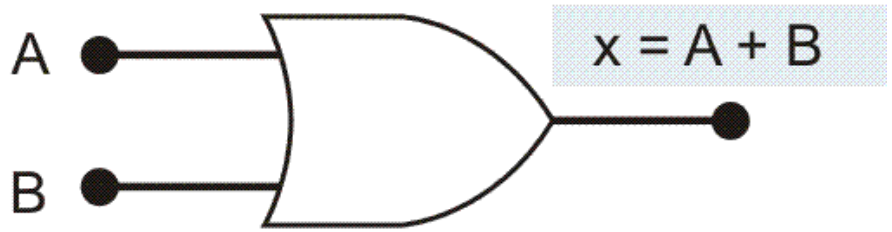
(c)

FIGURA 3-2 (a) Tabela-verdade que define a operação OR; (b) símbolo de uma porta OR de duas entradas.

OR

A	B	x = A + B
0	0	0
0	1	1
1	0	1
1	1	1

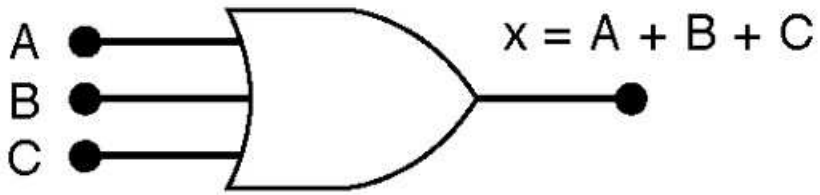
(a)



Porta OR

(b)

FIGURA 3-3 Símbolo e tabela-verdade para uma porta OR de três entradas.



A	B	C	x = A + B + C
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

FIGURA 3-4 Exemplo do uso de uma porta OR em um sistema de alarme.

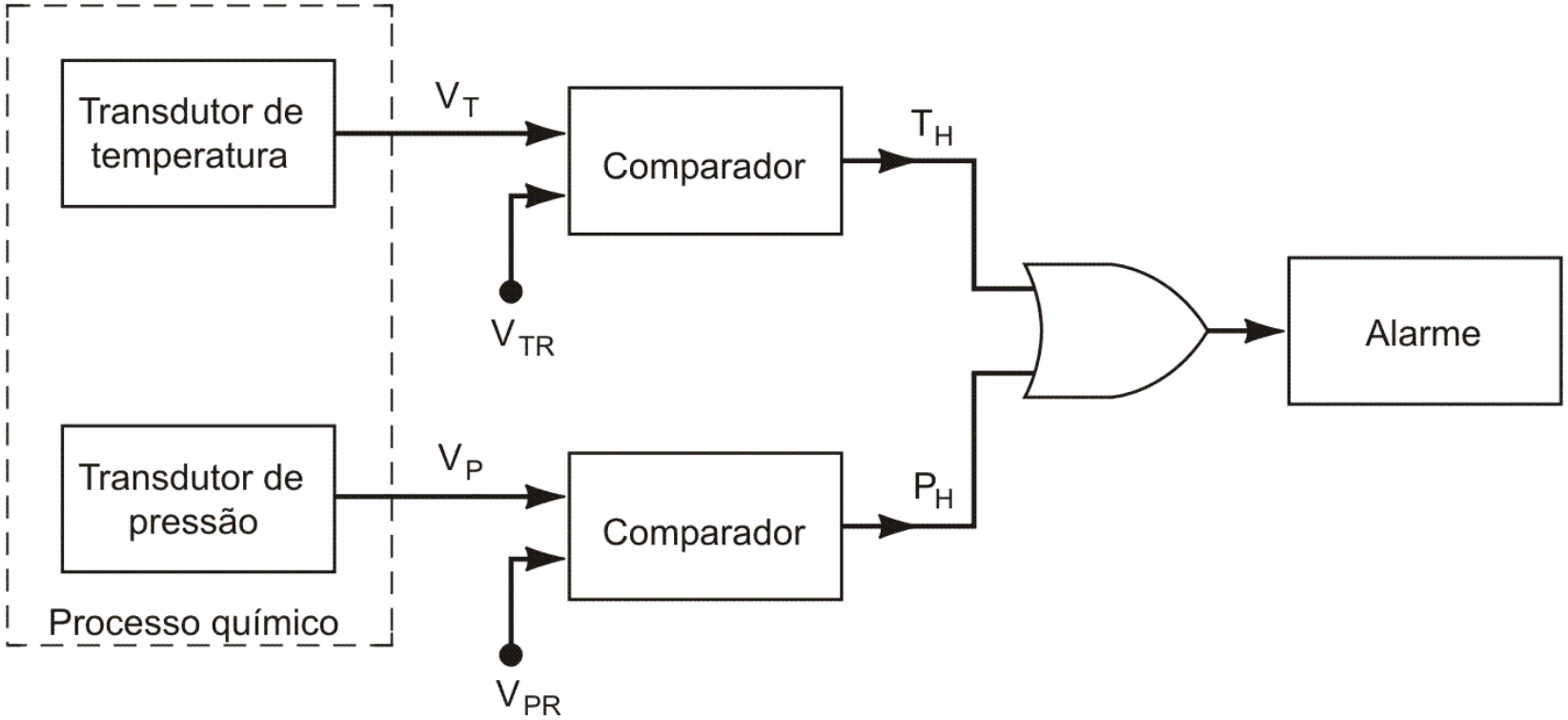
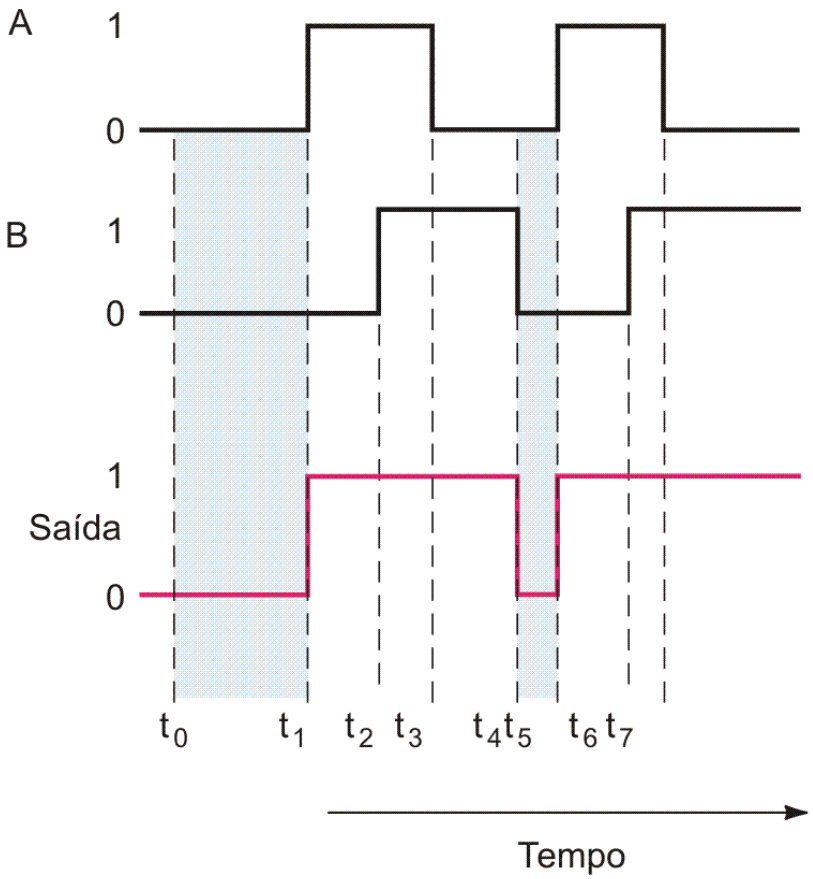


FIGURA 3-5 Exemplo 3-2.



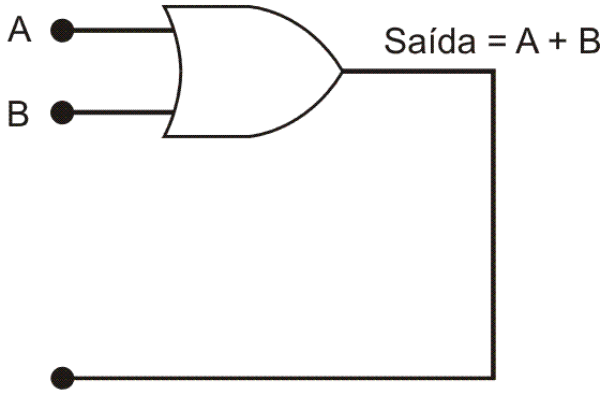
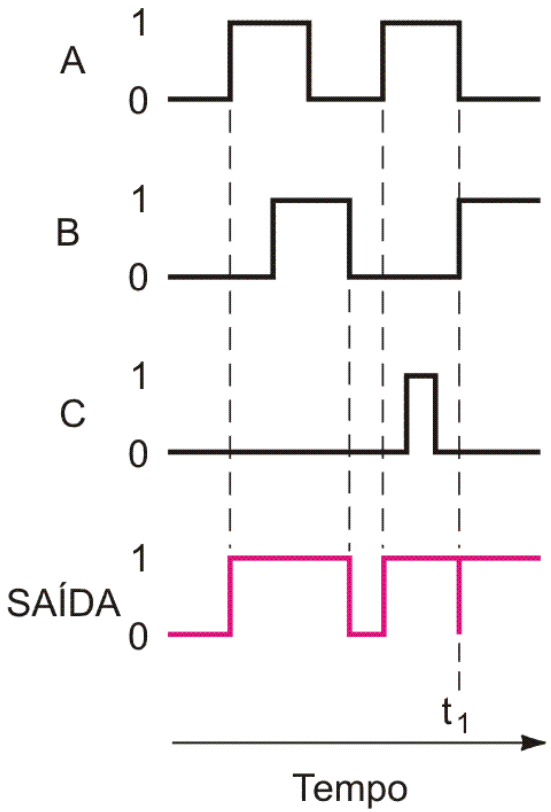


FIGURA 3-6 Exemplos 3-3a e 3-3b.



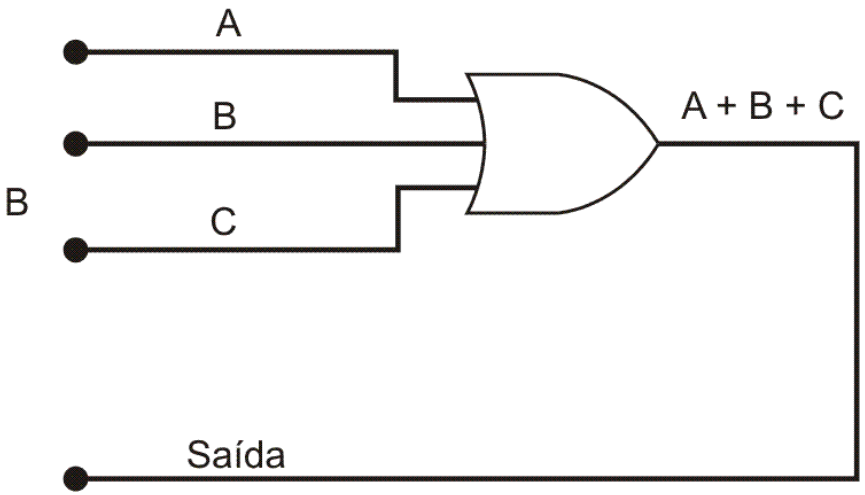
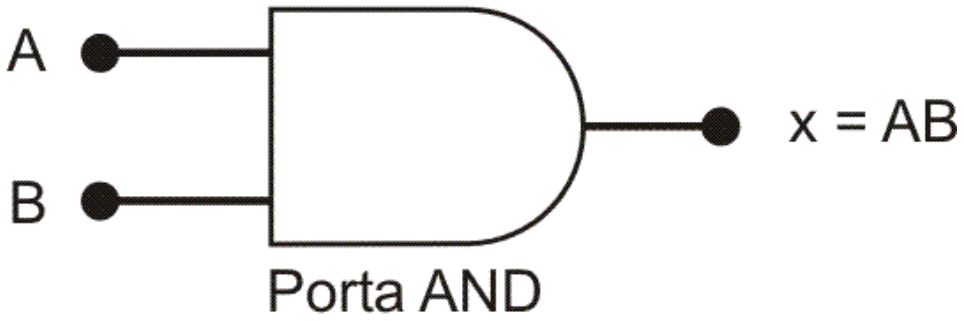


FIGURA 3-7 (a) Tabela-verdade para a operação AND; (b) símbolo da porta AND.

AND

A	B	x = A · B
0	0	0
0	1	0
1	0	0
1	1	1

(a)



(b)

FIGURA 3-8 Tabela-verdade e símbolo para uma porta AND de três entradas.

A	B	C	x = ABC
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

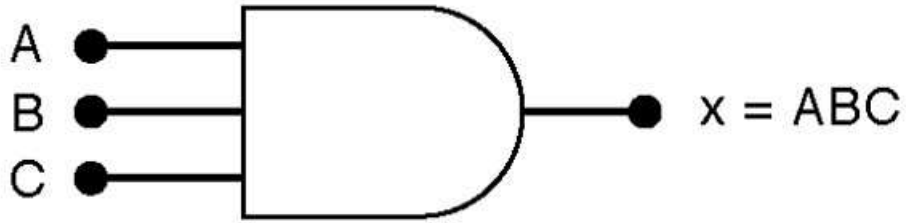


FIGURA 3-9 Exemplo 3-4.

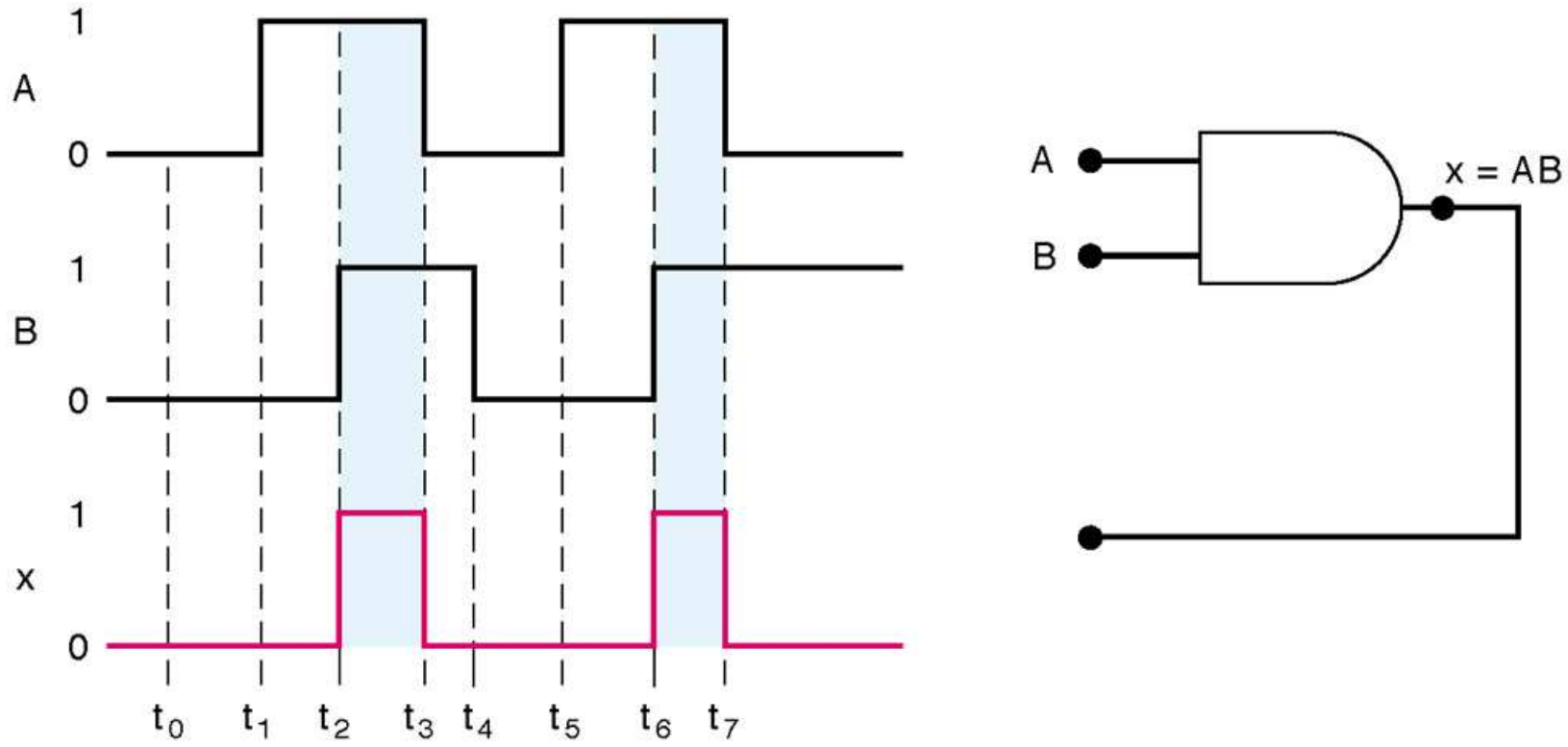


FIGURA 3-10 Exemplos 3-5a e 3-5b.

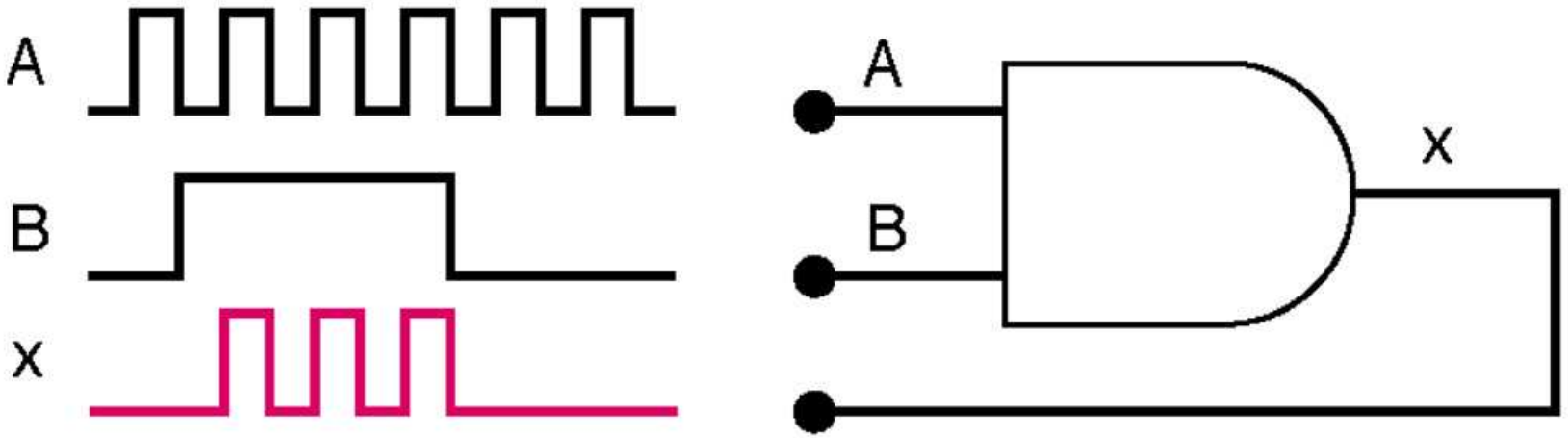


FIGURA 3-11 (a) Tabela-verdade; (b) símbolo para o INVERSOR (circuito NOT); (c) exemplos de formas de ondas.

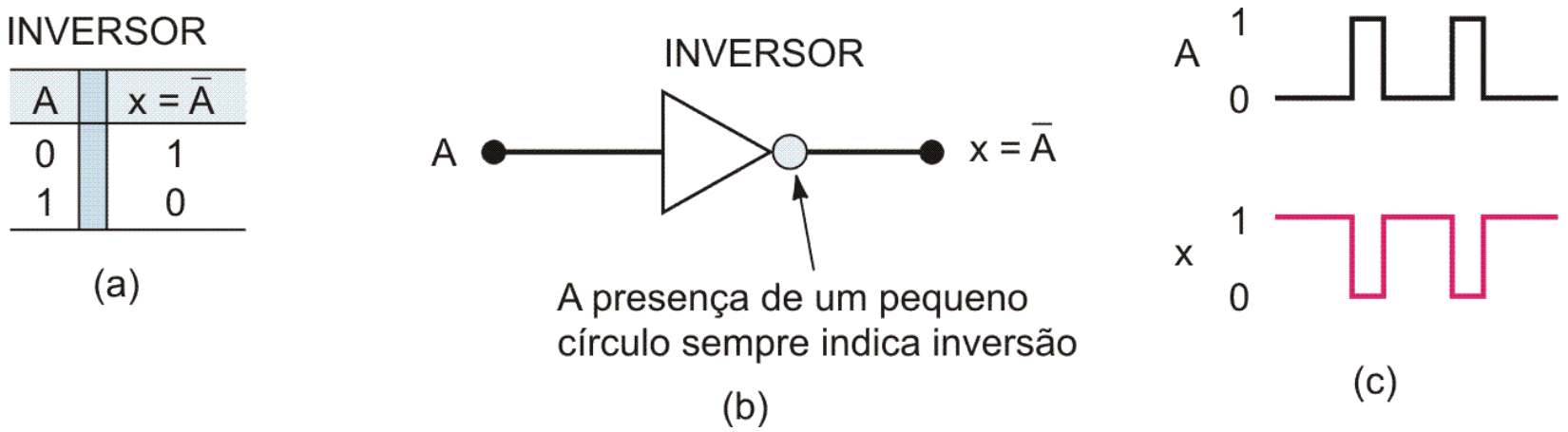


FIGURA 3-12 Um cirduito lógico e suas expressões Booleanas.

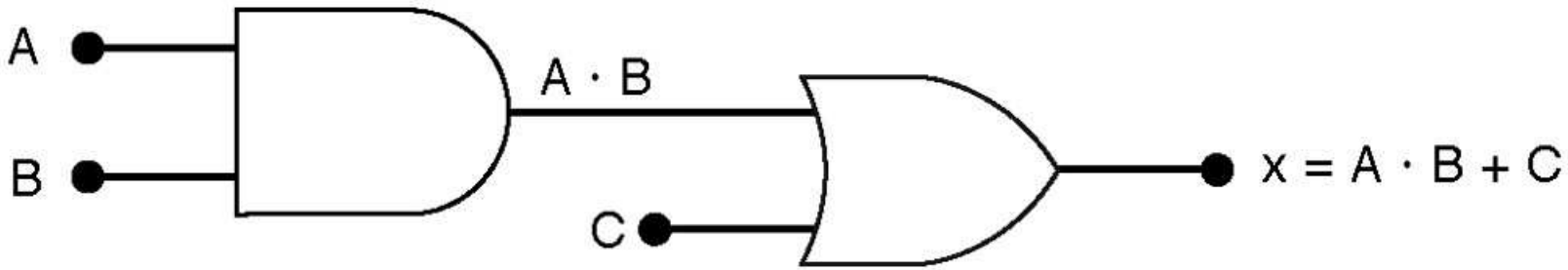


FIGURA 3-13 Circuito lógico cuja expressão requer parênteses.

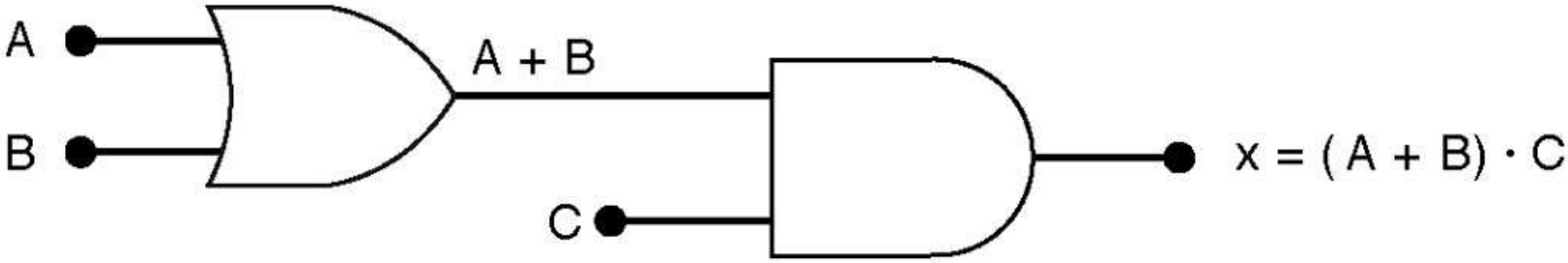


FIGURA 3-14 Circuitos com INVERSORES.

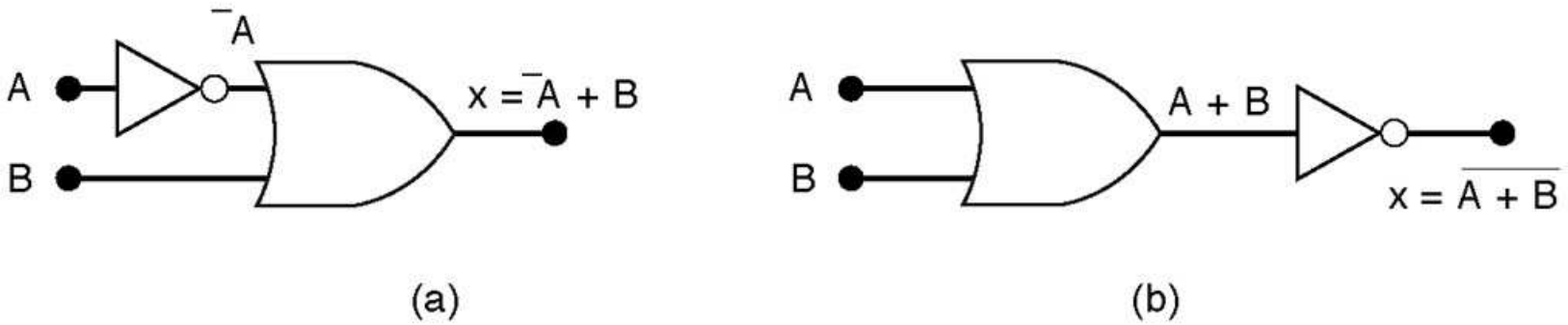


FIGURA 3-15 Mais exemplos.

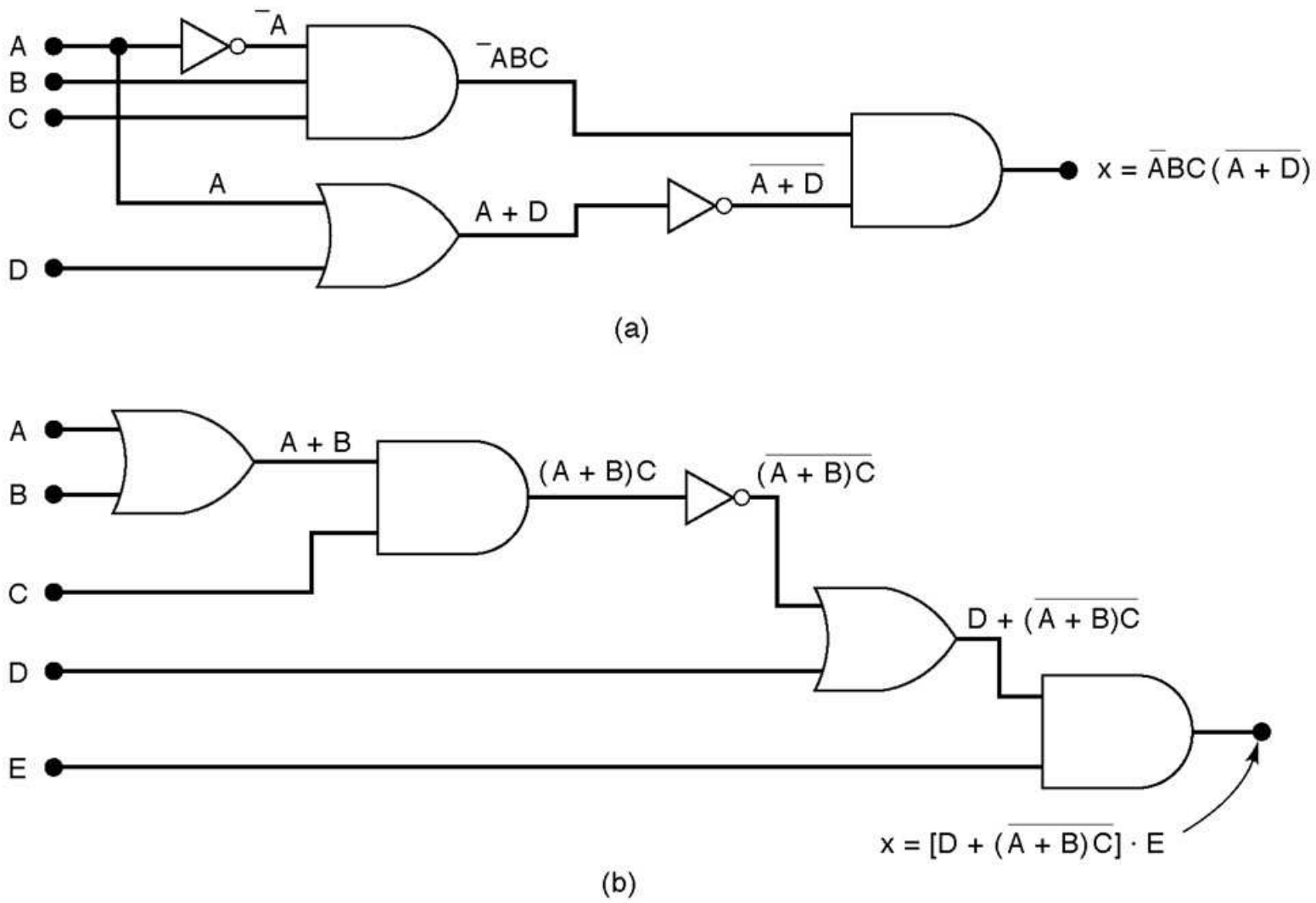


FIGURA 3-16 Determinando o nível lógico da saída a partir de um diagrama do circuito.

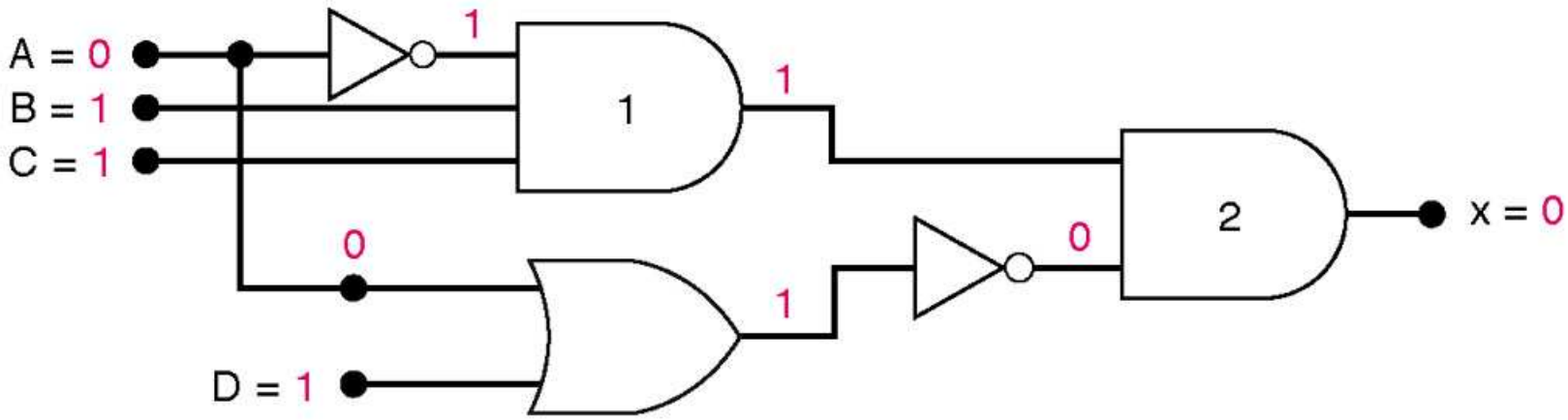


FIGURA 3-17 Constuindo um circuito lógico a partir de uma expressão Booleana.

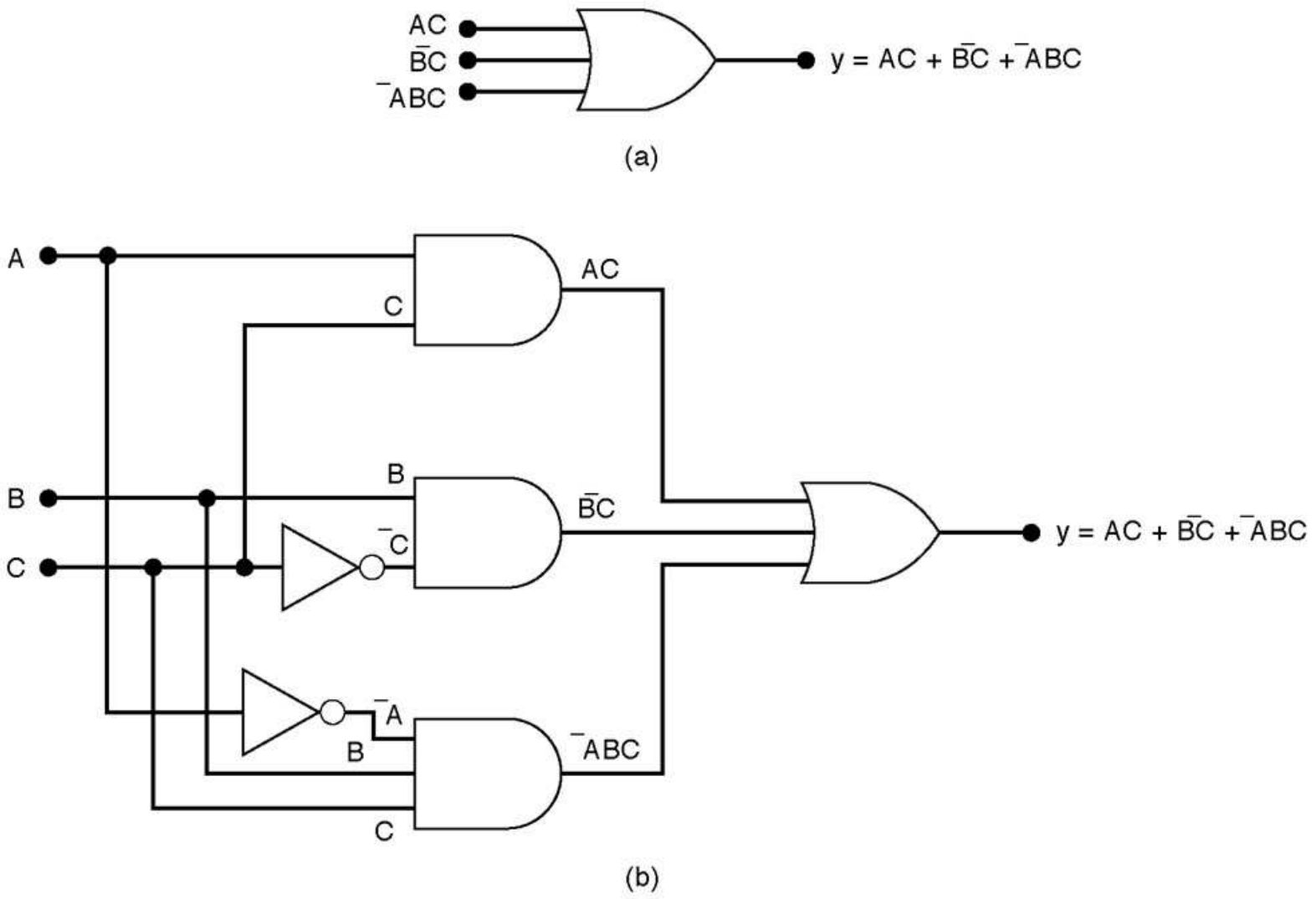


FIGURA 3-18 Exemplo 3-7.

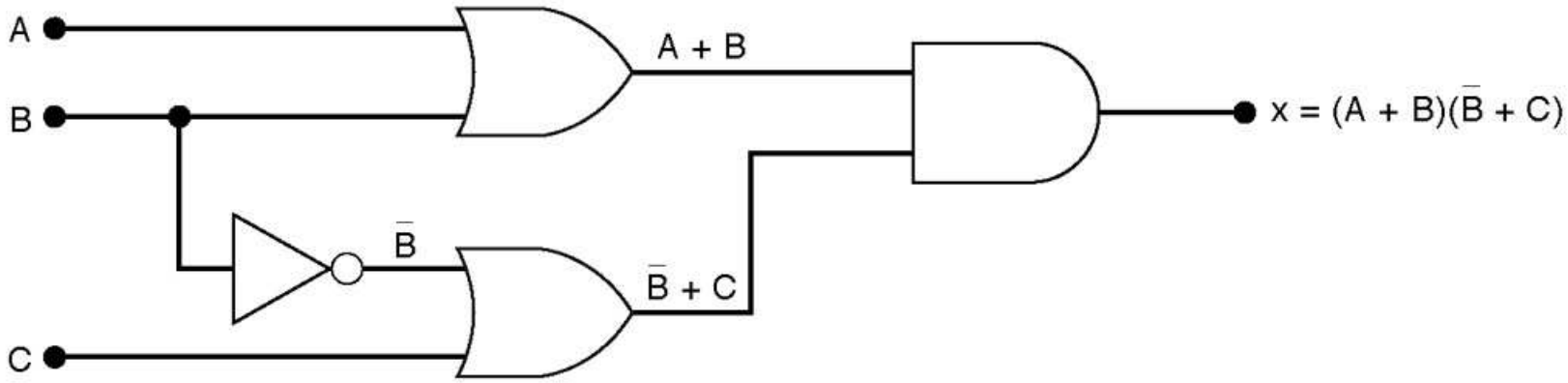
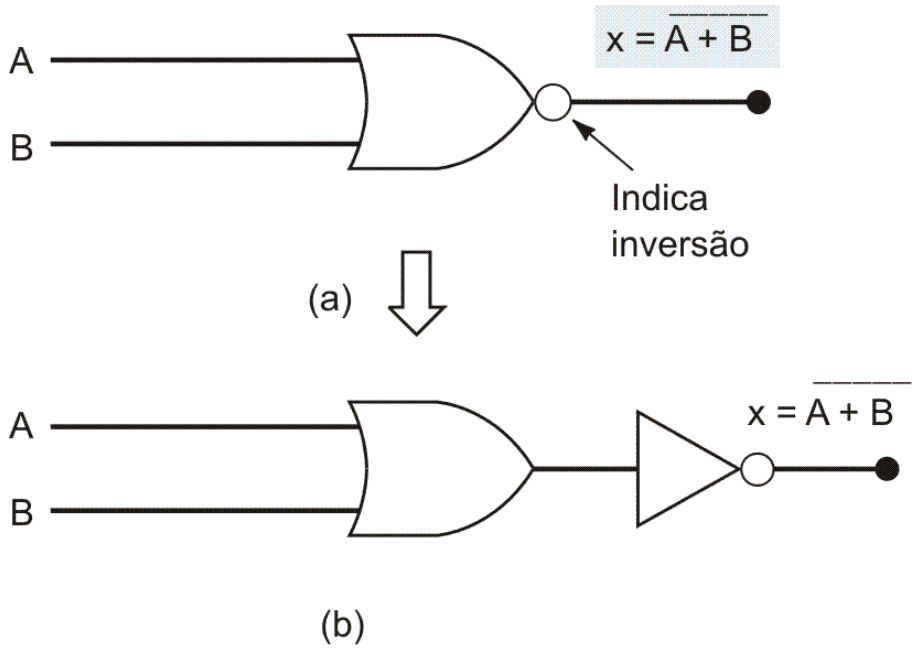


FIGURA 3-19 (a) Símbolo de porta NOR; (b) Circuito equivalente; (c) Tabela-verdade.



		OR	NOR
A	B	A + B	$\overline{A + B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

(c)

FIGURA 3-20 Exemplo 3-8.

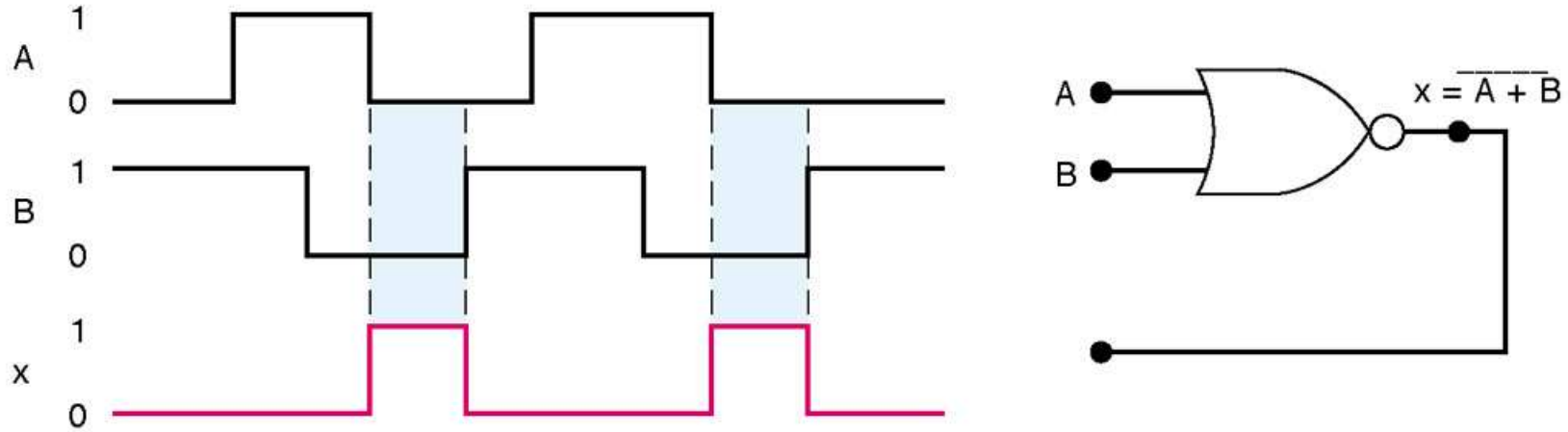


FIGURA 3-21 Exemplo 3-9.

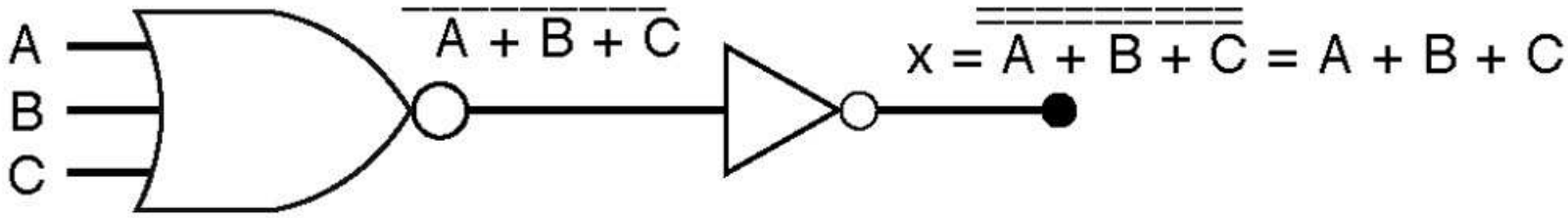
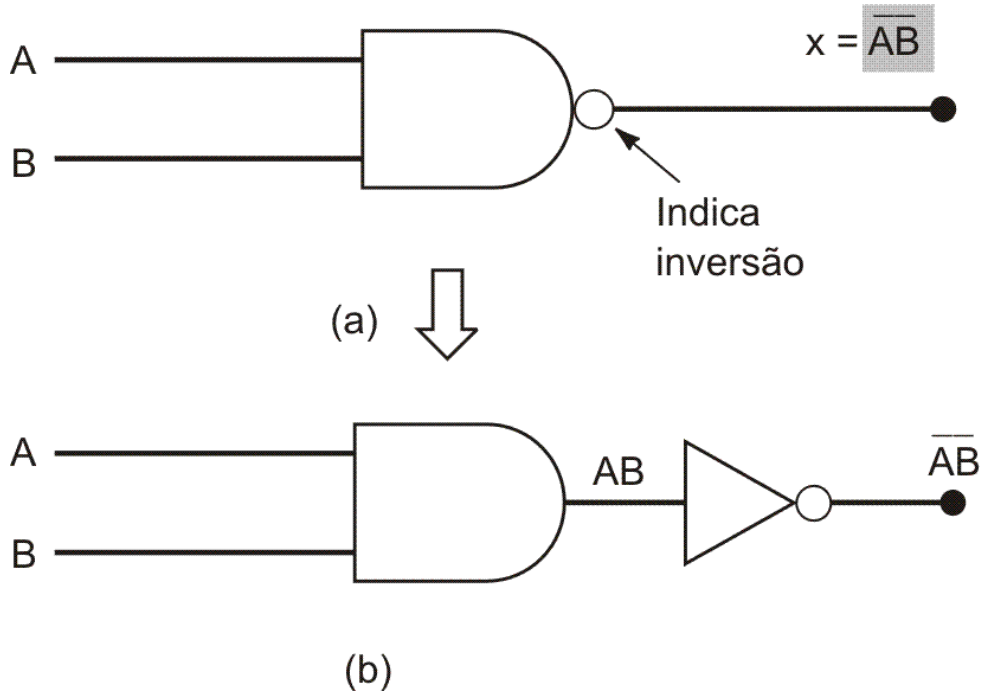


FIGURA 3-22 (a) Símbolo da porta NAND; (b) Circuito equivalente; (c) Tabela-verdade .



		AND	NAND
A	B	AB	$\overline{AB}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

(c)

FIGURA 3-23 Exemplo 3-10.

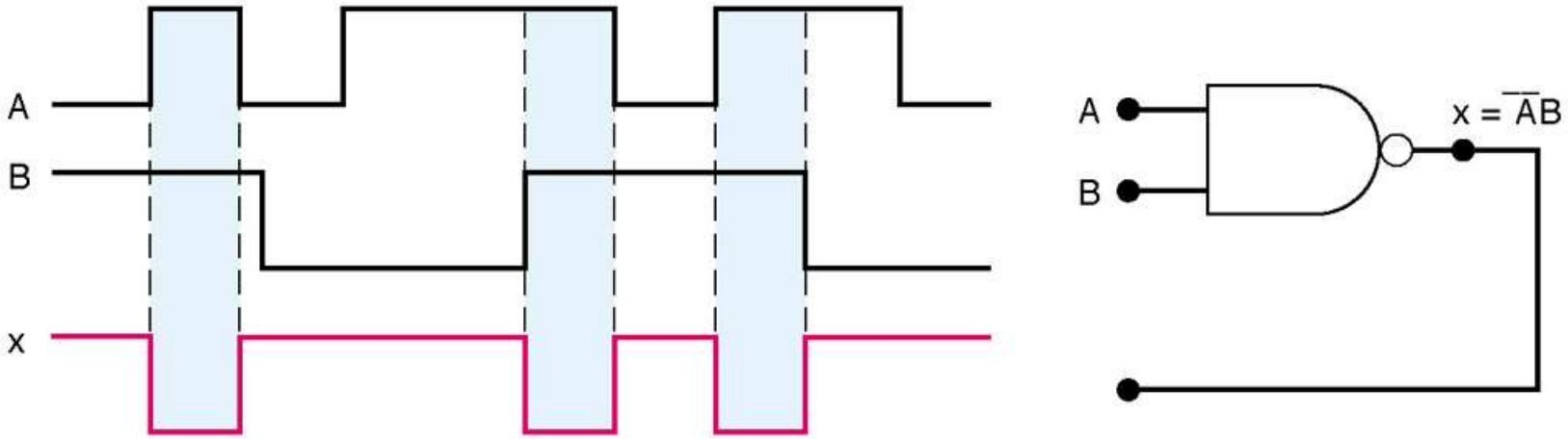


FIGURA 3-24 Exemplos 3-11 e 3-12.

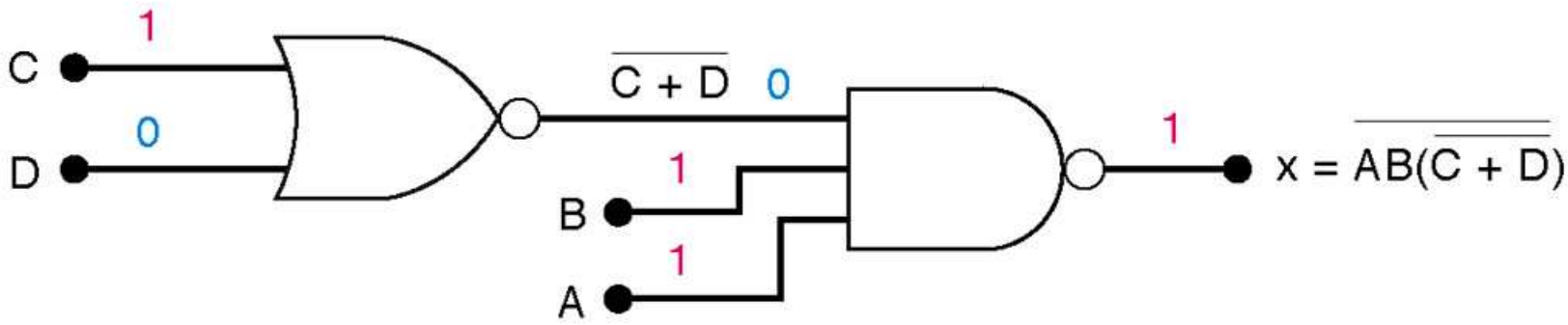


FIGURA 3-25 Teoremas para uma única variável.

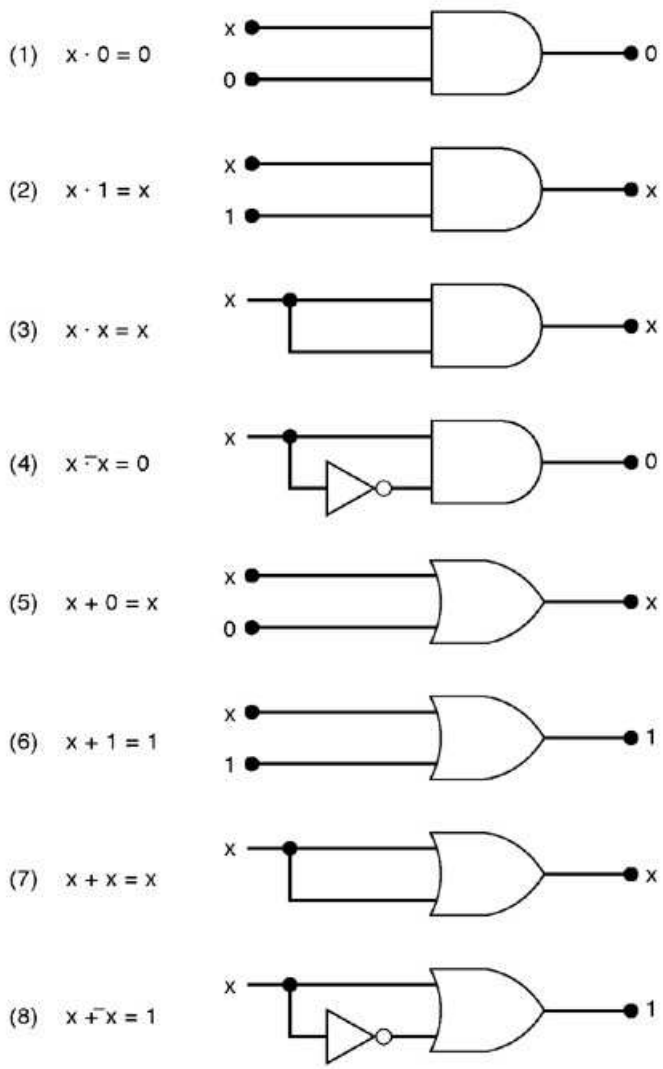
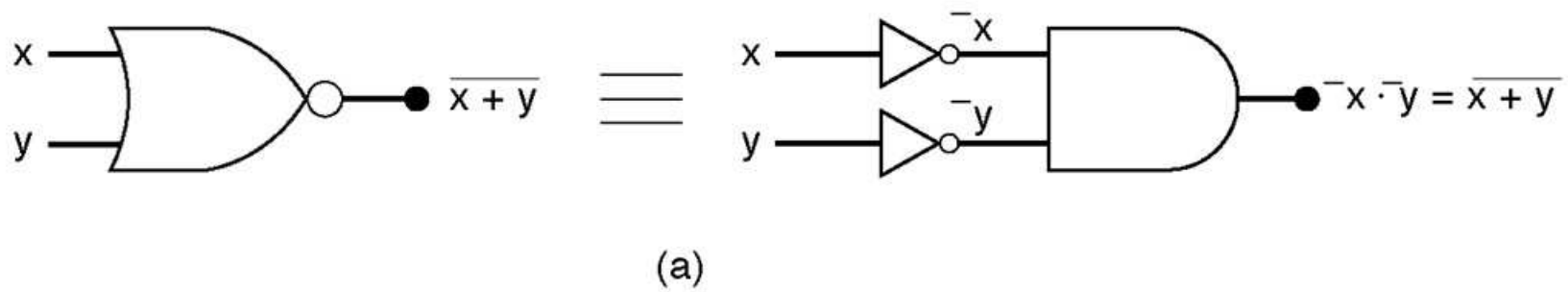
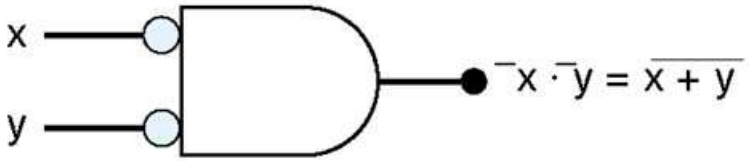


FIGURA 3-26 (a) Circuitos equivalentes relativos ao teorema (16); (b) símbolo alternativo para a função NOR.



(a)



(b)

FIGURA 3-27 (a) Circuitos equivalentes relativos ao teorema (17); (b) símbolo alternativo para a função NAND.

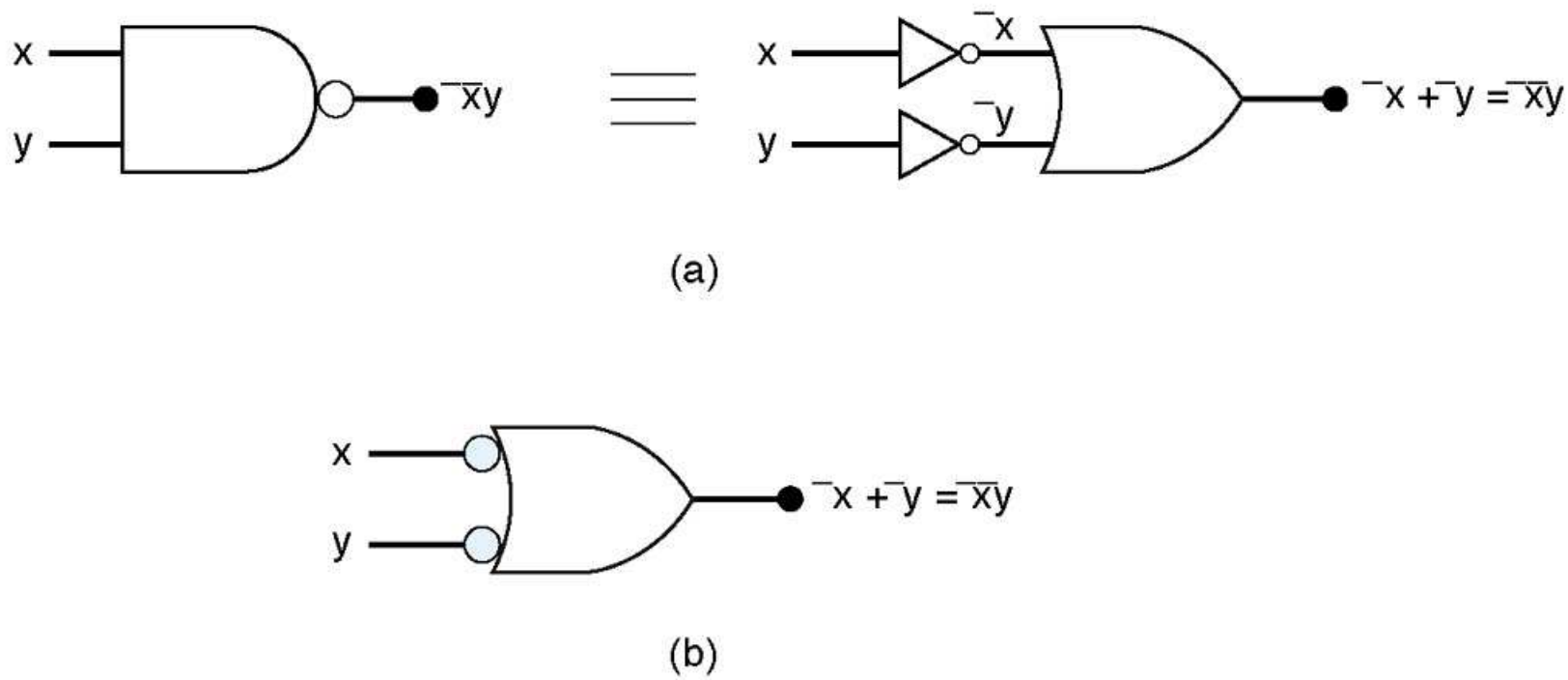


FIGURA 3-28 Exemplo 3-17.

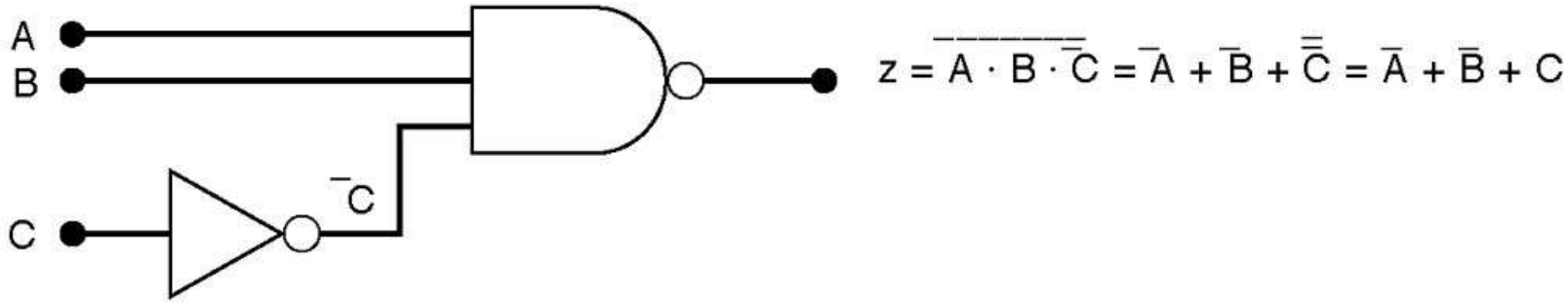


FIGURA 3-29 As portas NAND podem ser usadas para implementar qualquer função booleana.

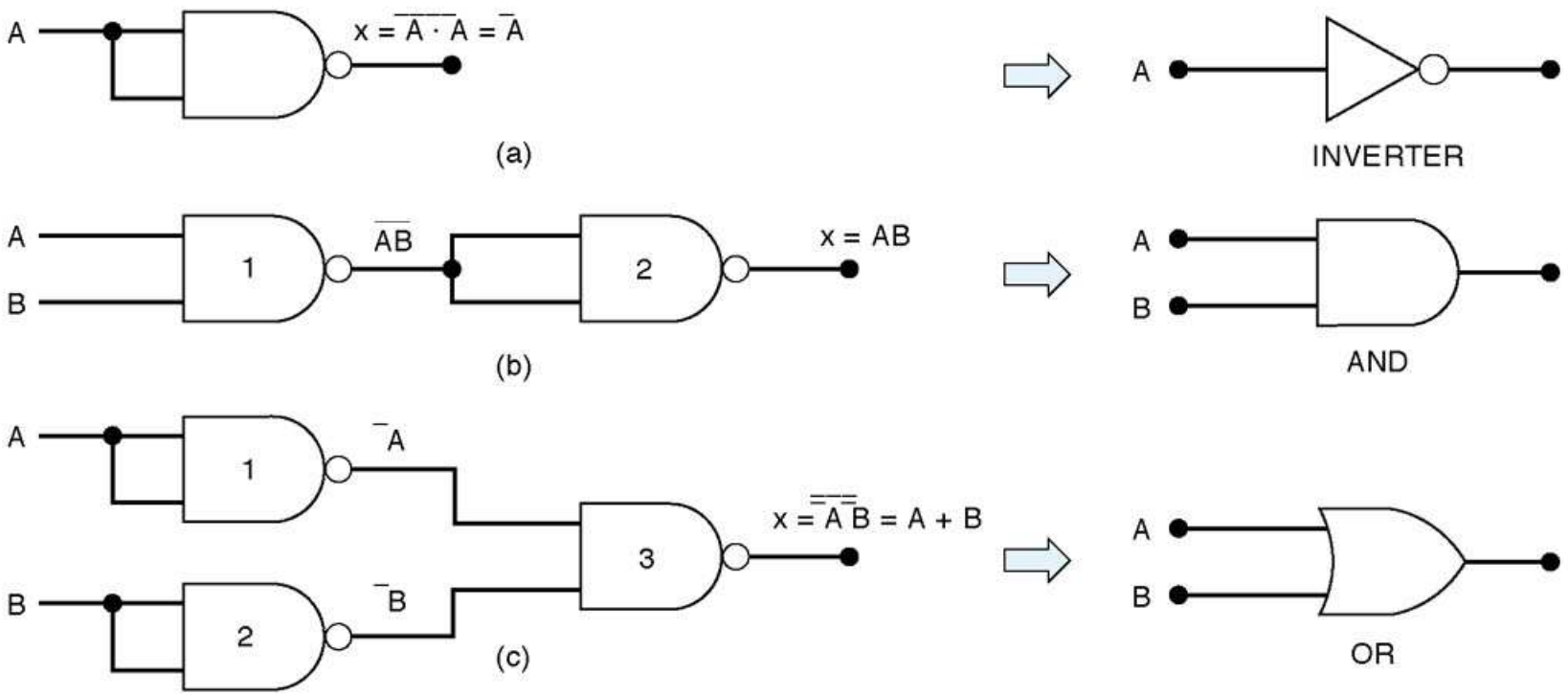


FIGURA 3-30 As portas NOR podem ser usadas para implementar qualquer operação booleana.

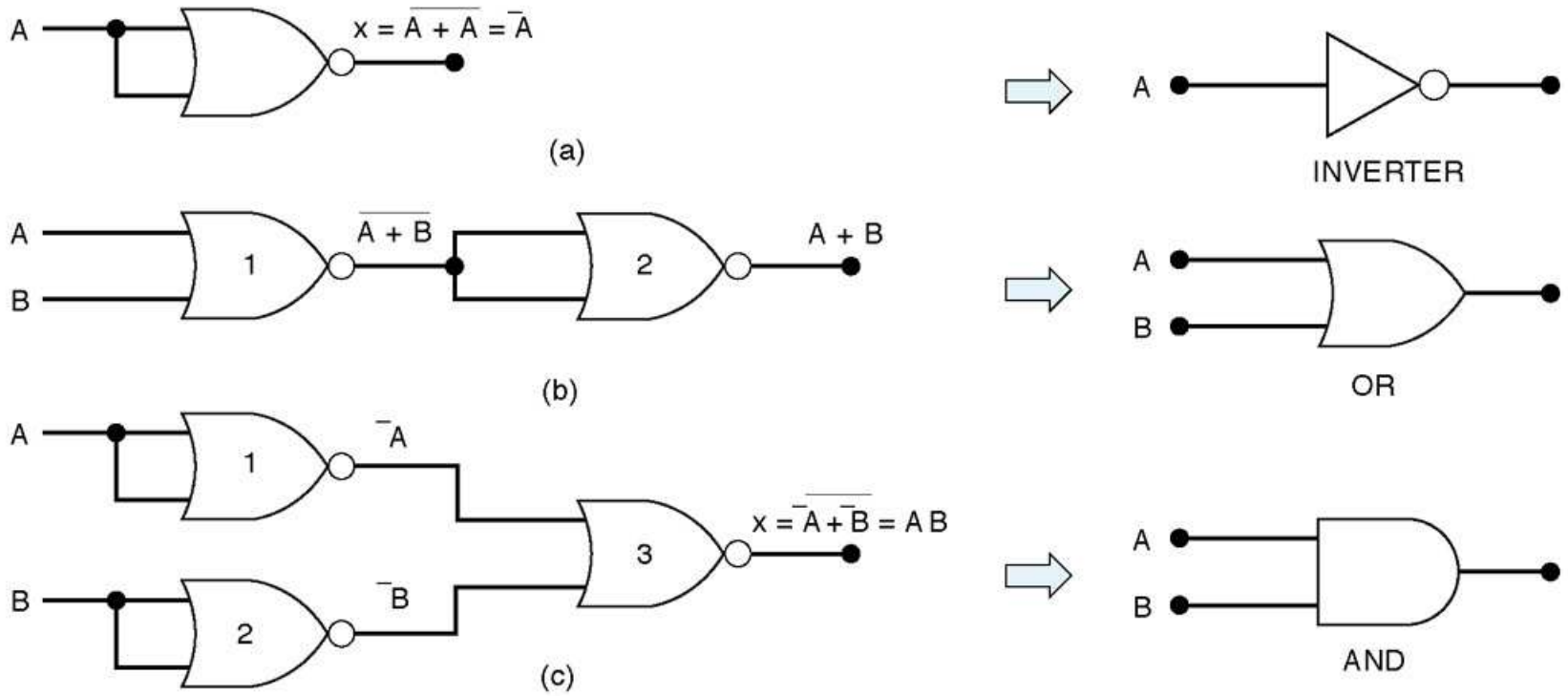


FIGURA 3-31 CIs disponíveis para o Exemplo 3-18.

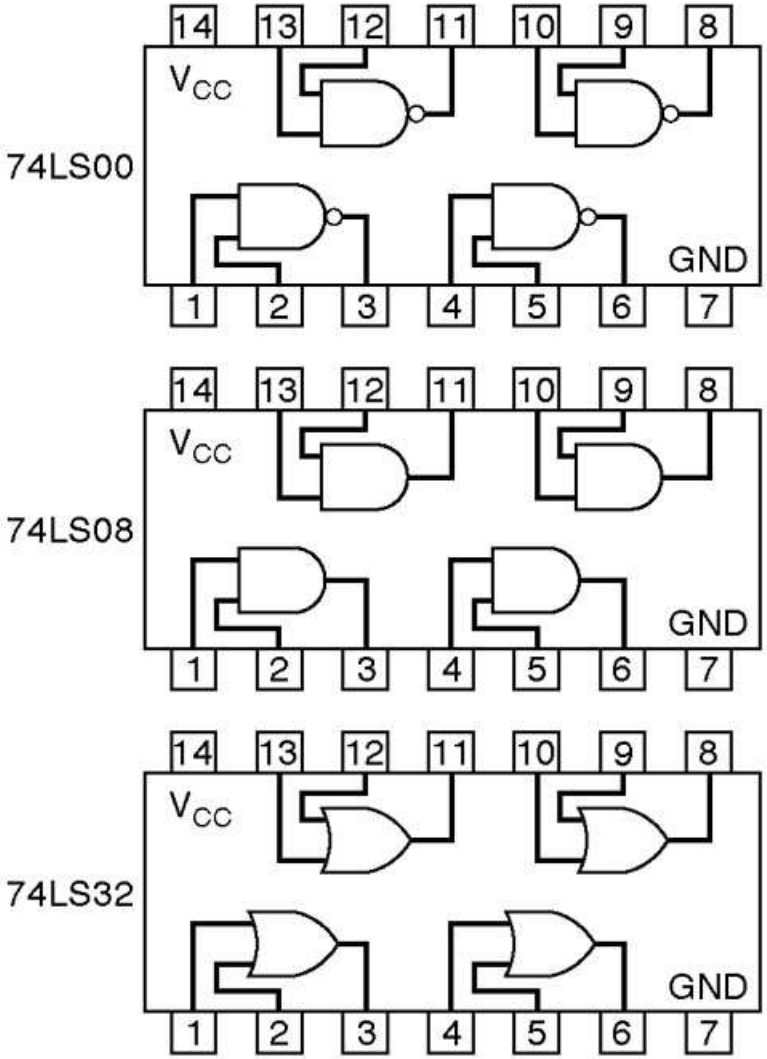


FIGURA 3-32 Implementações possíveis para Exemplo 3-18.

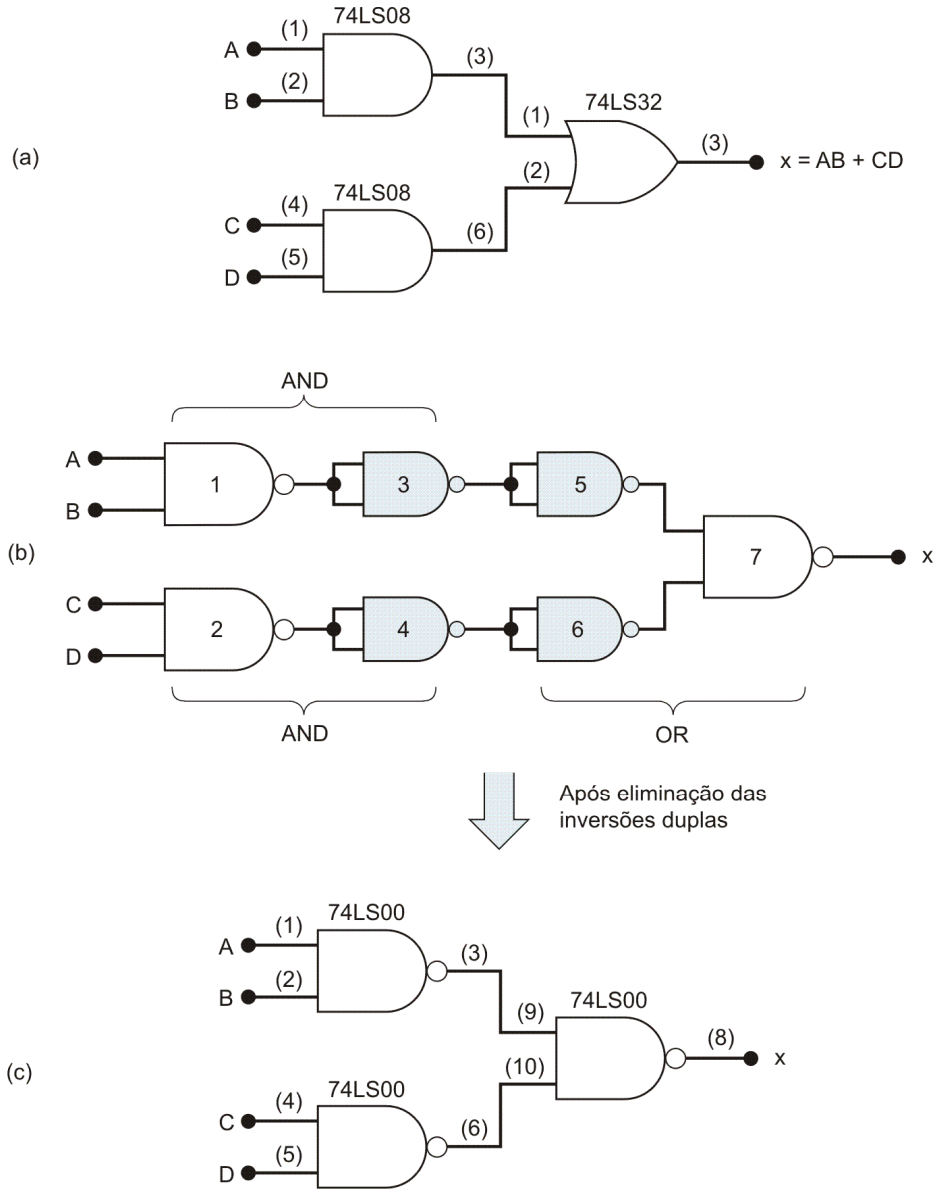


FIGURA 3-33 Simbolos-padrão e alternativos para várias portas lógicas e para o inversor.

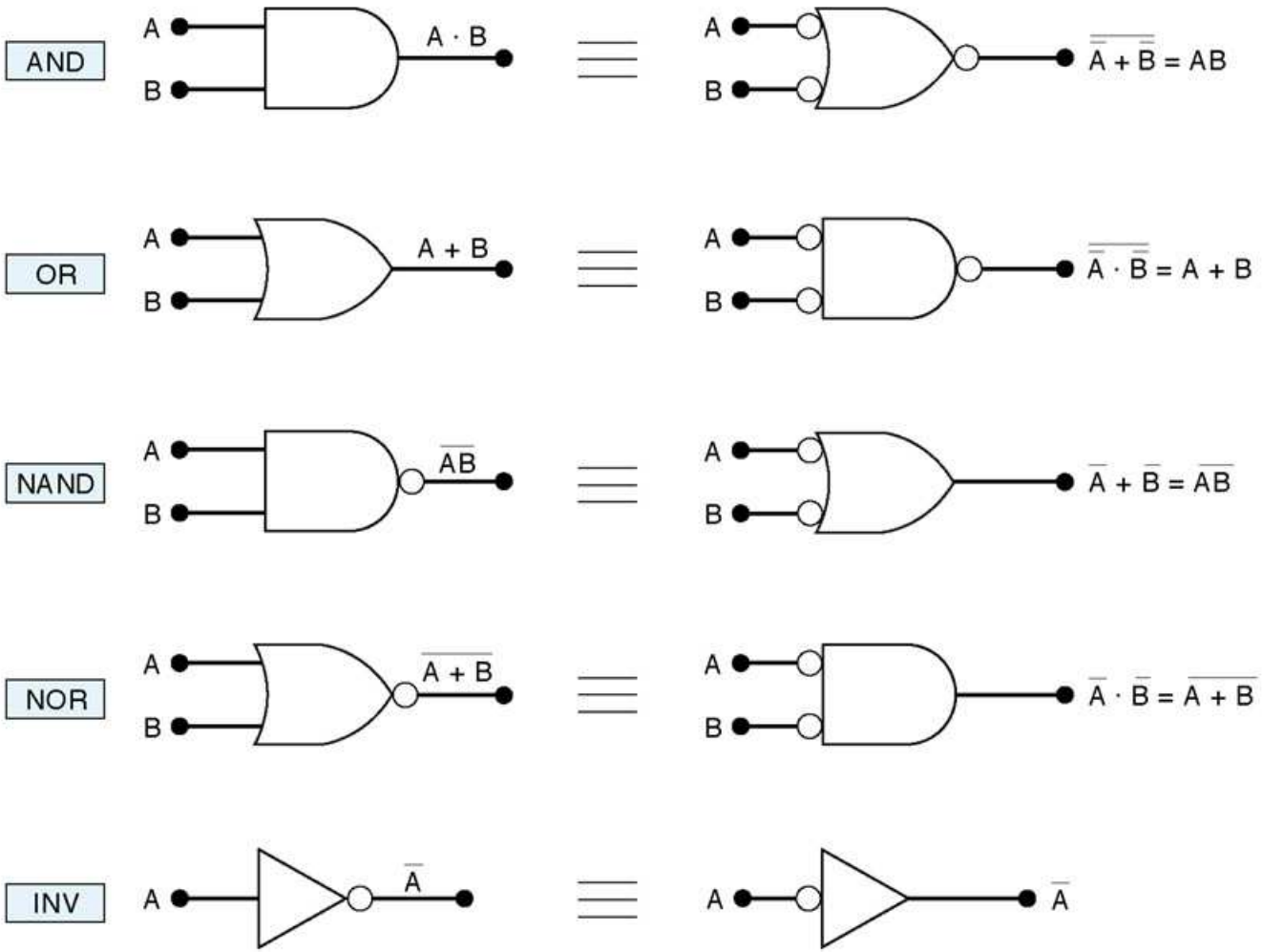
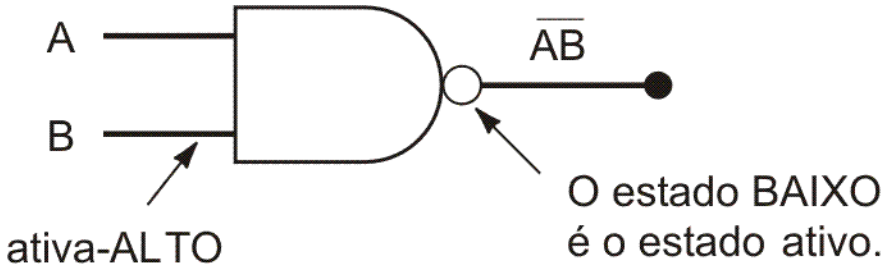
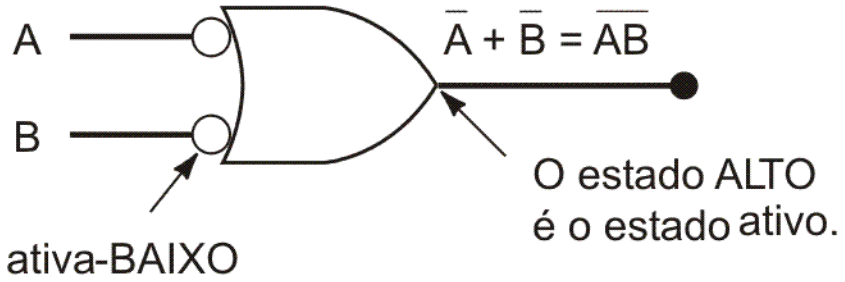


FIGURA 3-34 Interpretação dos dois símbolos da porta NAND.



A saída vai para o nível BAIXO apenas quando todas as entradas forem para o nível ALTO.

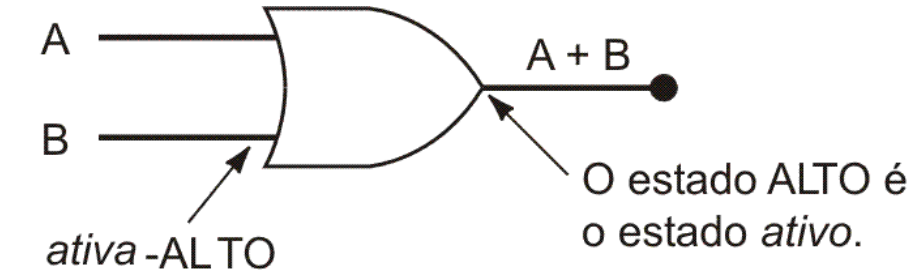
(a)



A saída vai para o nível ALTO quando qualquer entrada for para o nível BAIXO.

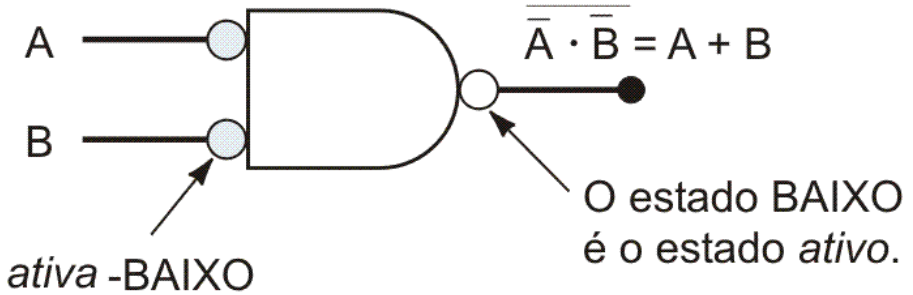
(b)

FIGURA 3-35 Interpretação dos dois símbolos da porta OR.



A saída vai para o nível BAIXO quando todas as entradas forem para o nível BAIXO.

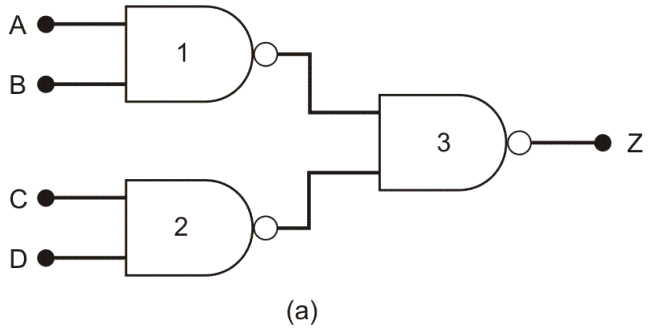
(a)



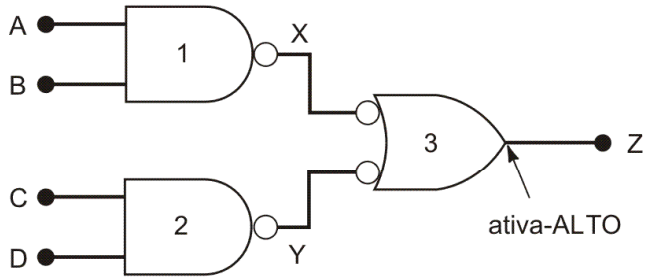
A saída vai para o nível ALTO quando qualquer entrada for para o nível ALTO.

(b)

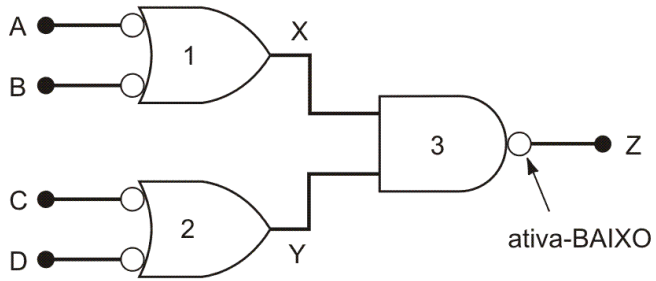
FIGURA 3-36 (a) Circuito original usando símbolos-padrão NAND; (b)Representação equivalente em que a saída Z é ativa-ALTO; (c) Representação equivalente em que a saída Z é ativa-BAIXO; (d) Tabela-verdade.



(a)



(b)



(c)

A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

(d)

FIGURA 3-37 Exemplo 3-20.

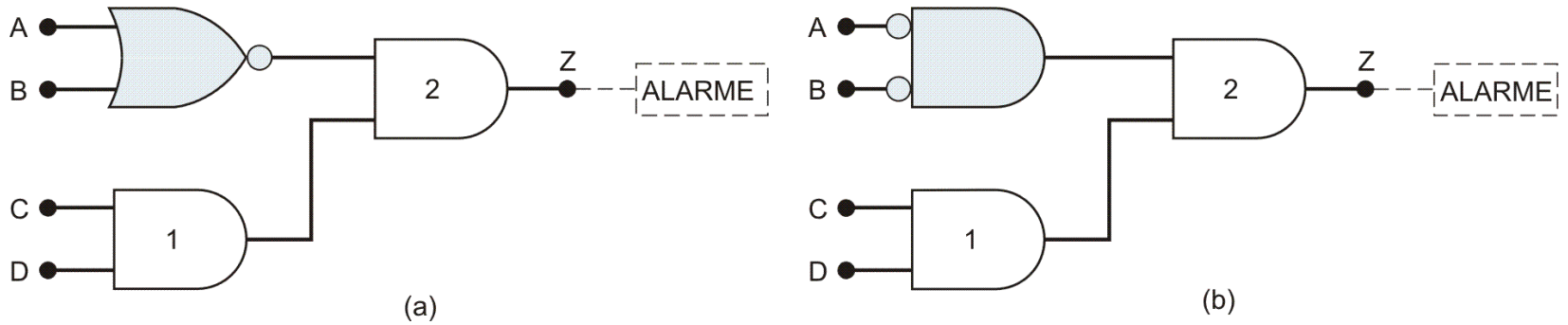


FIGURA 3-38 Exemplo 3-21.

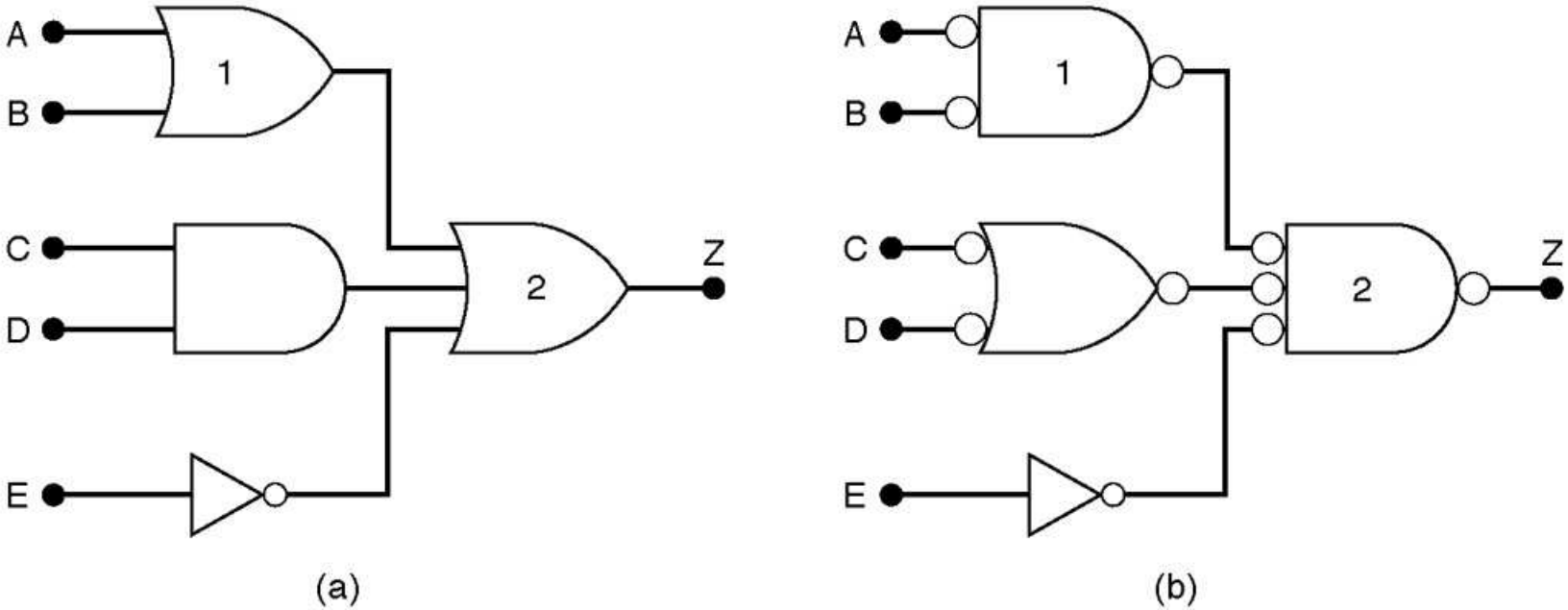


FIGURA 3-39 Exemplo 3-22.

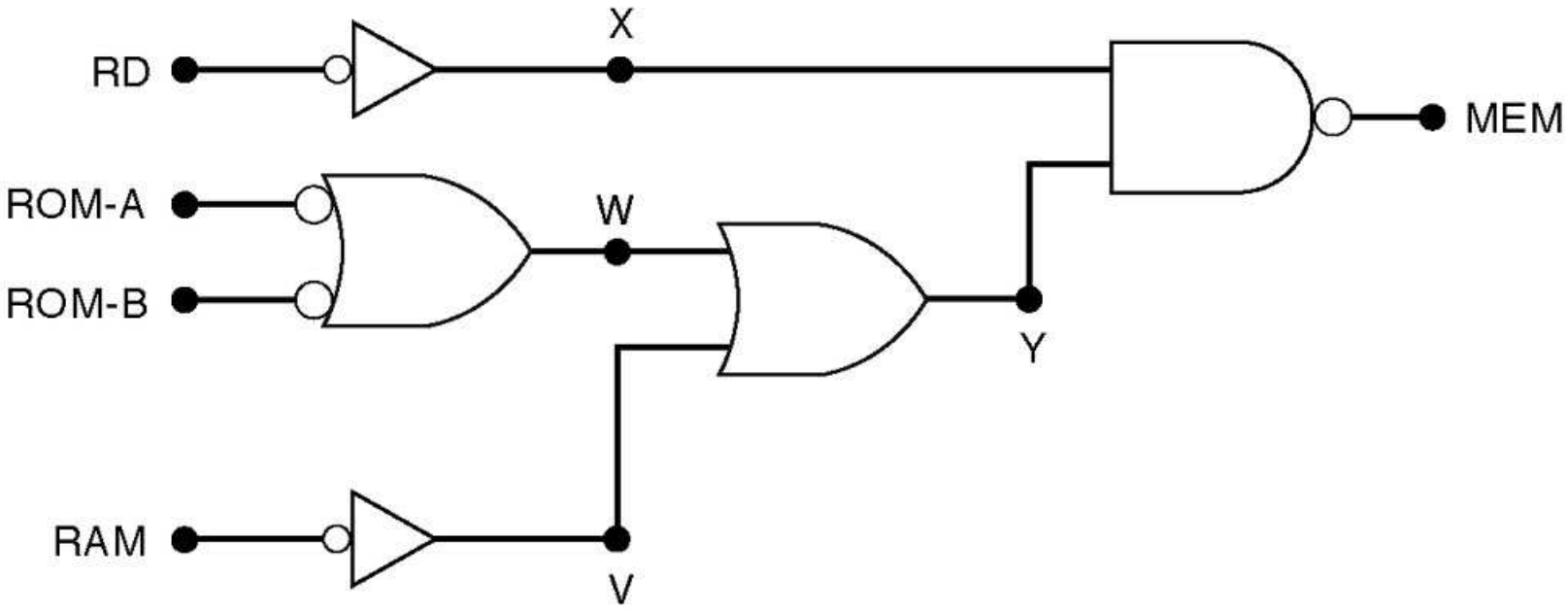


FIGURA 3-40 Exemplo 3-23.

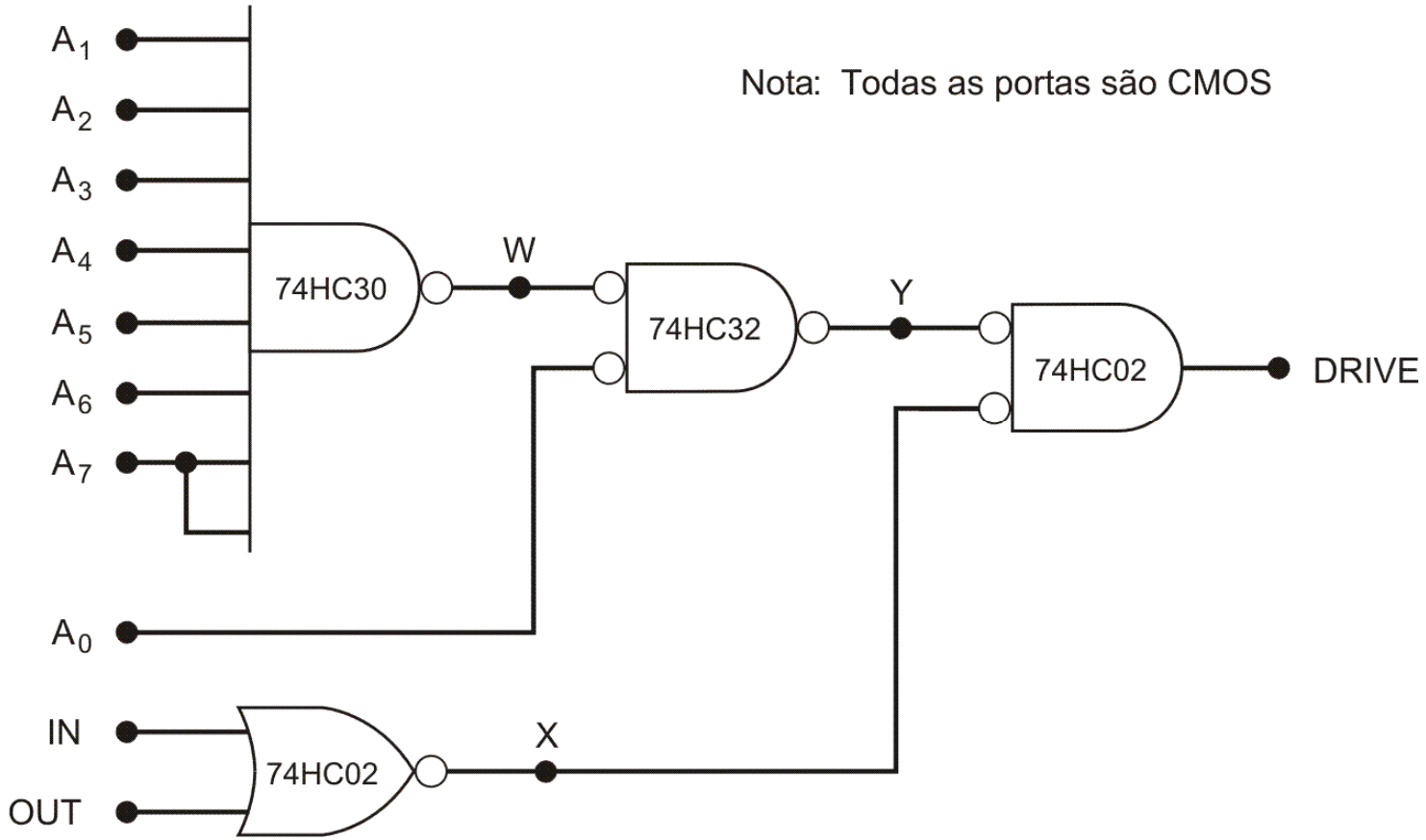


FIGURA 3-41 Símbolos lógicos-padrão: (a) tradicional; (b) IEEE/ANSI.

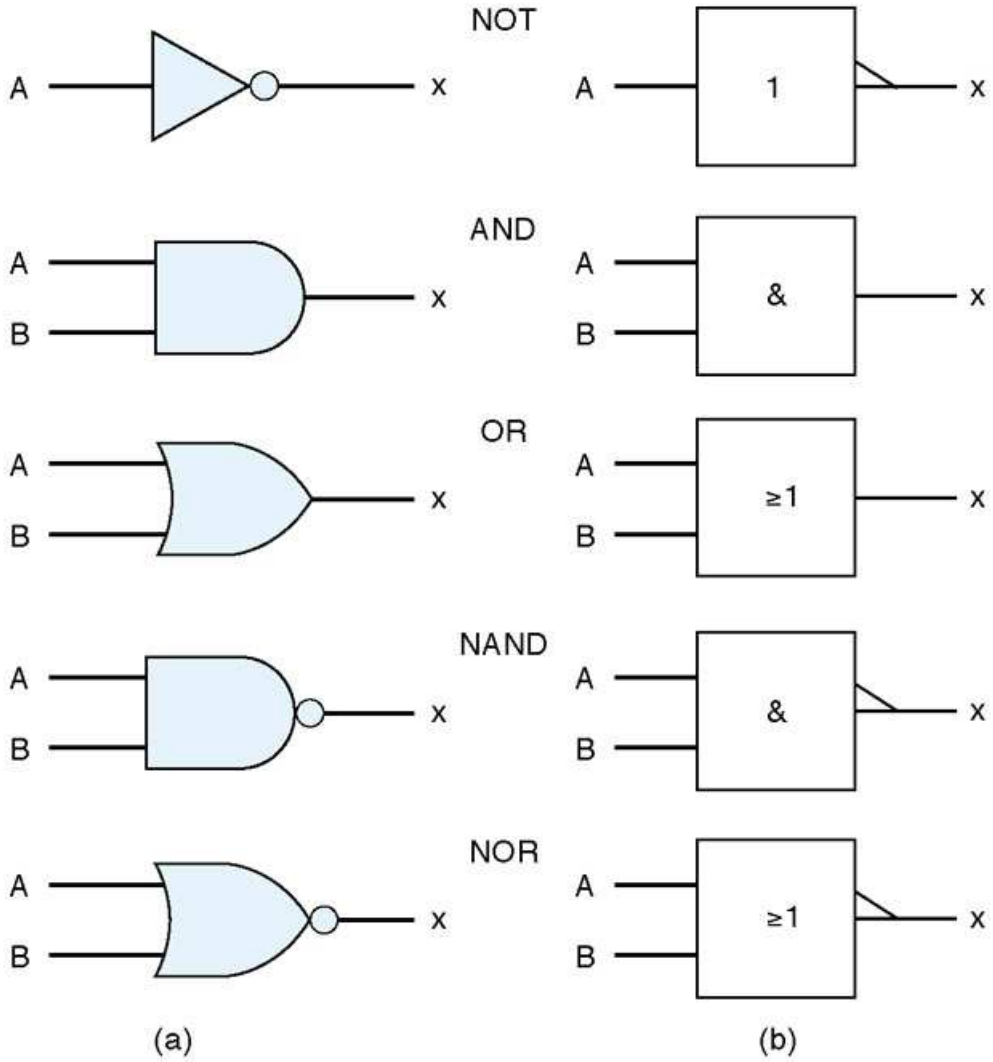


FIGURA 3-42

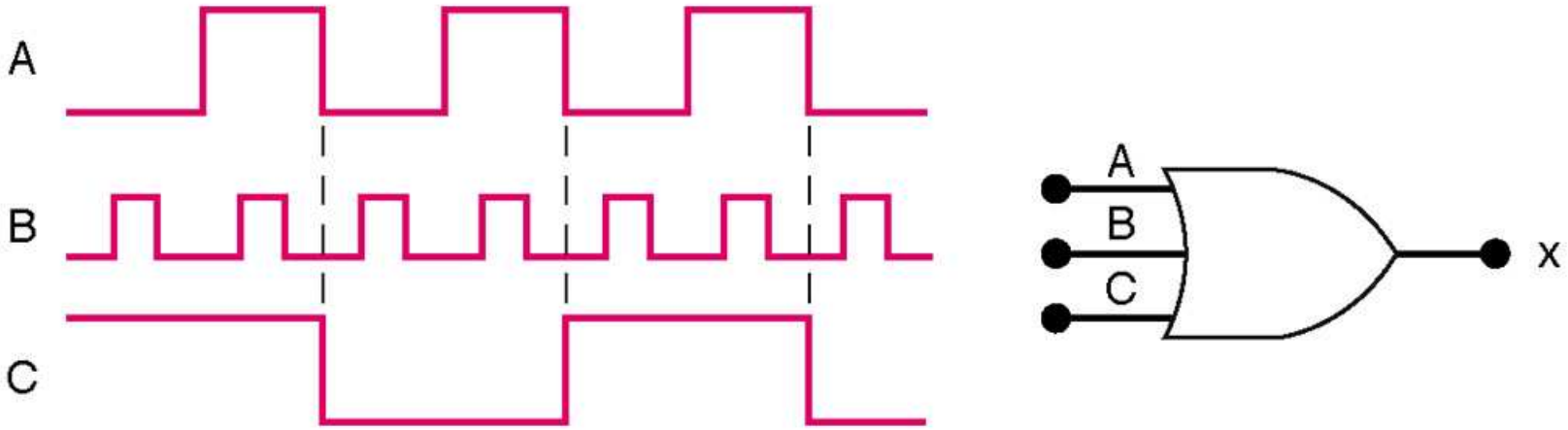


FIGURA 3-43

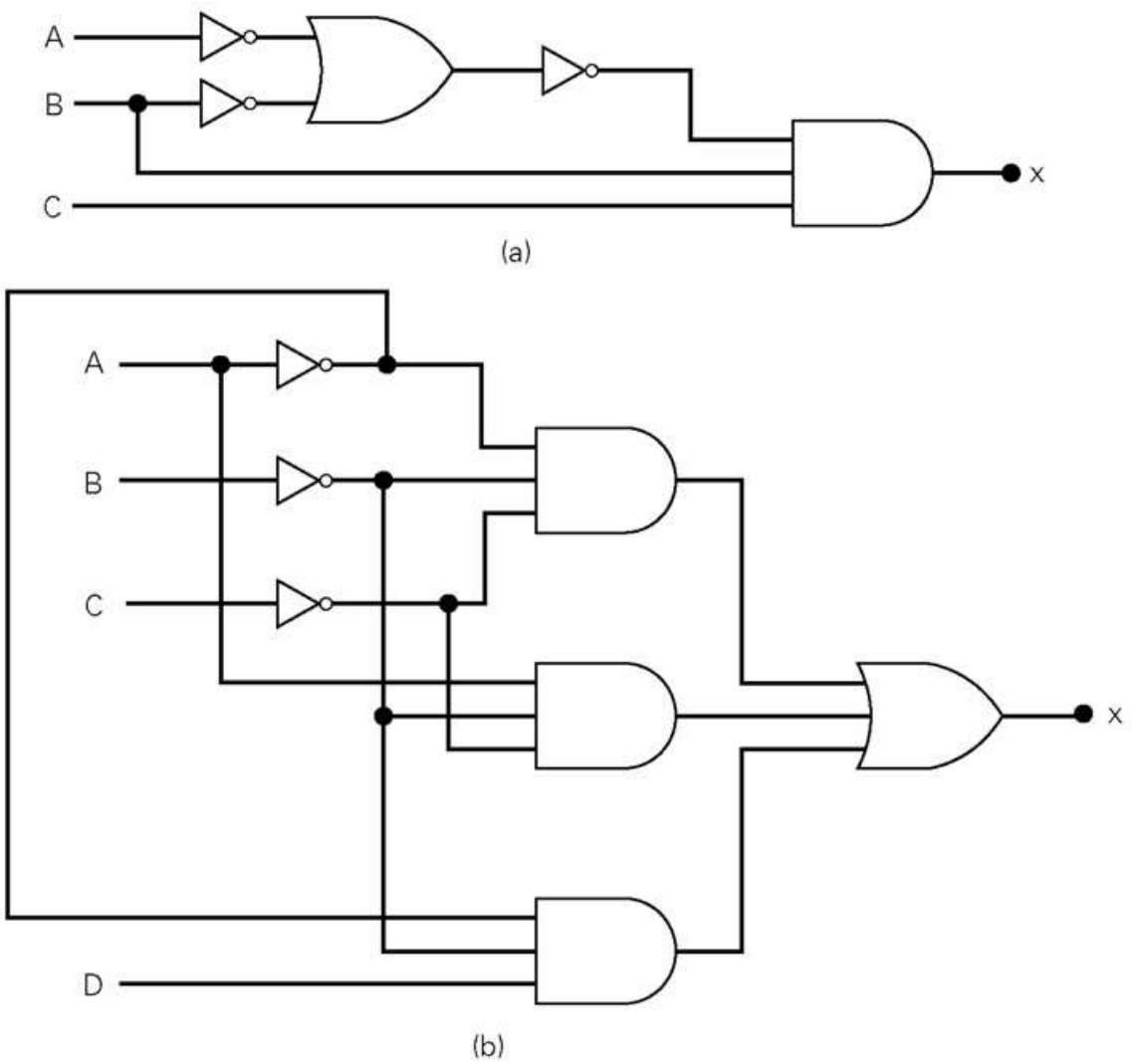


FIGURA 3-44

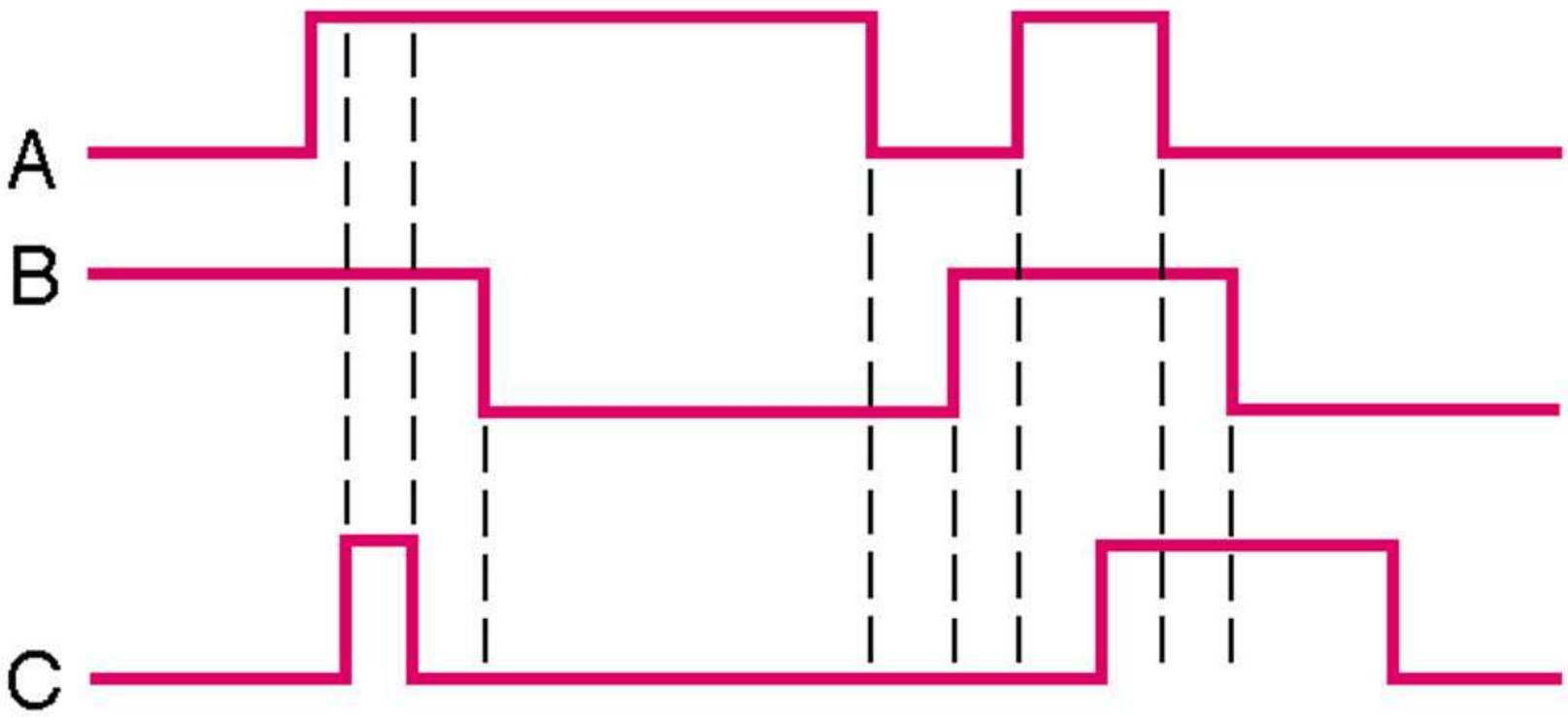


FIGURA 3-45

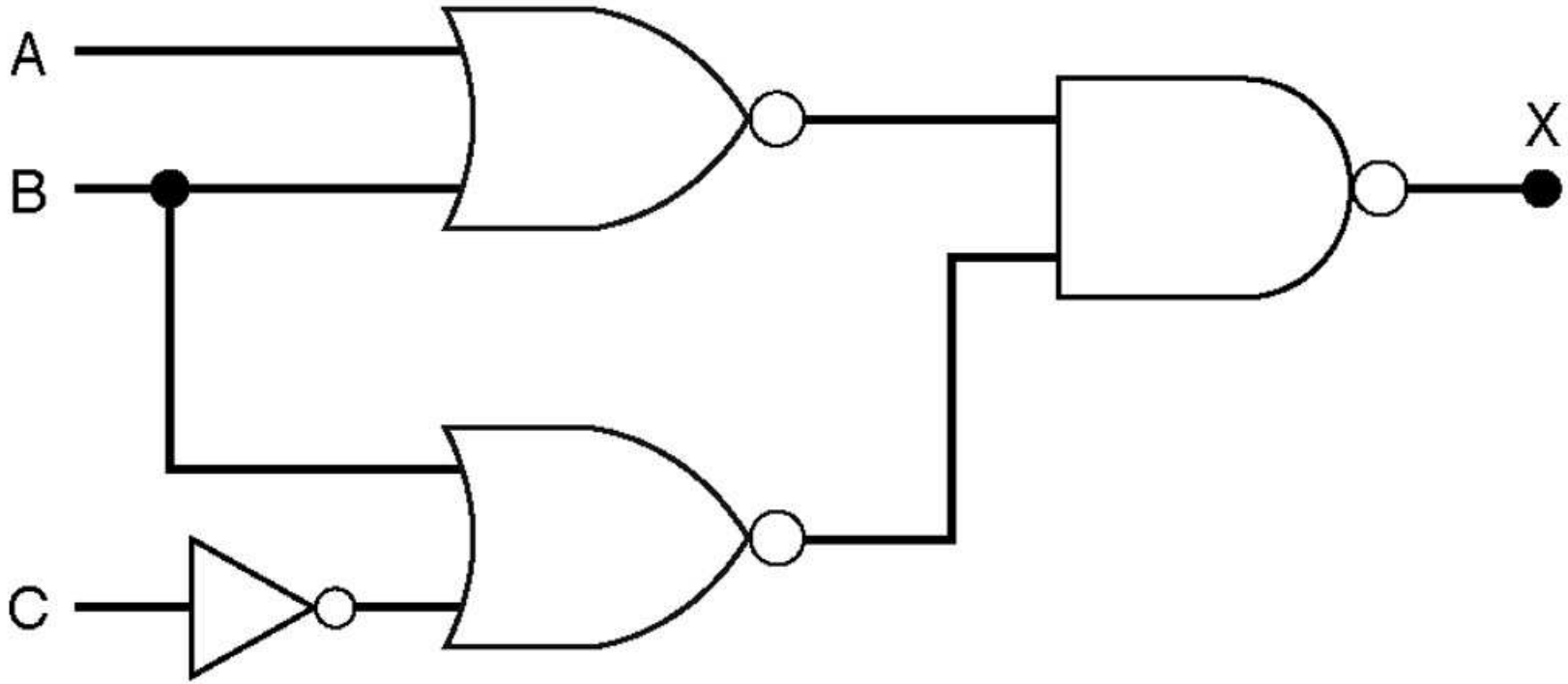


FIGURA 3-46

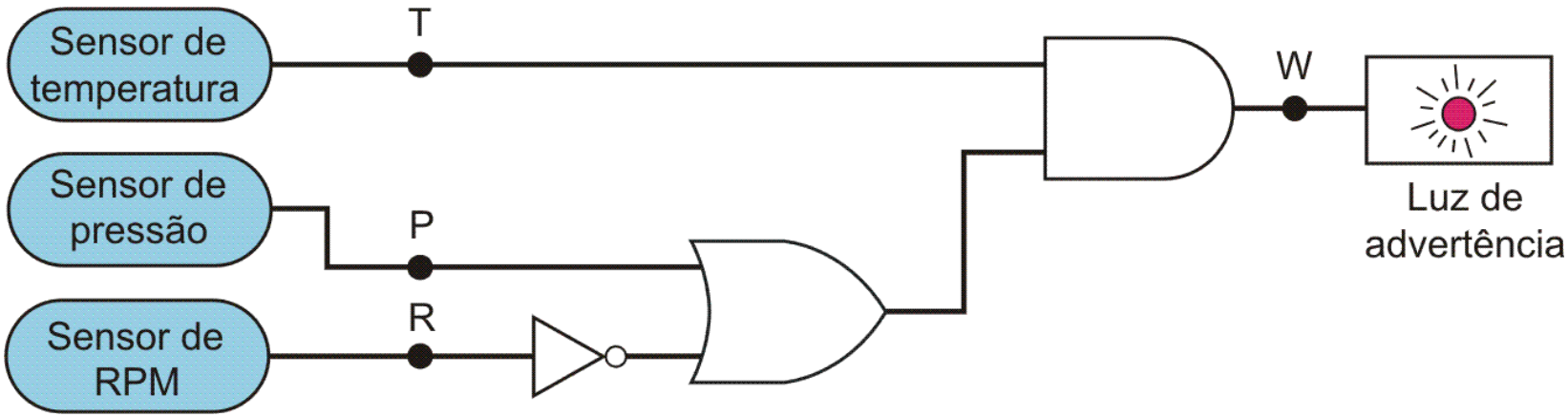

Sensor de temperatura
Sensor de pressão
Sensor de RPM
T
P
R
W
Luz de advertência

FIGURA 3-47

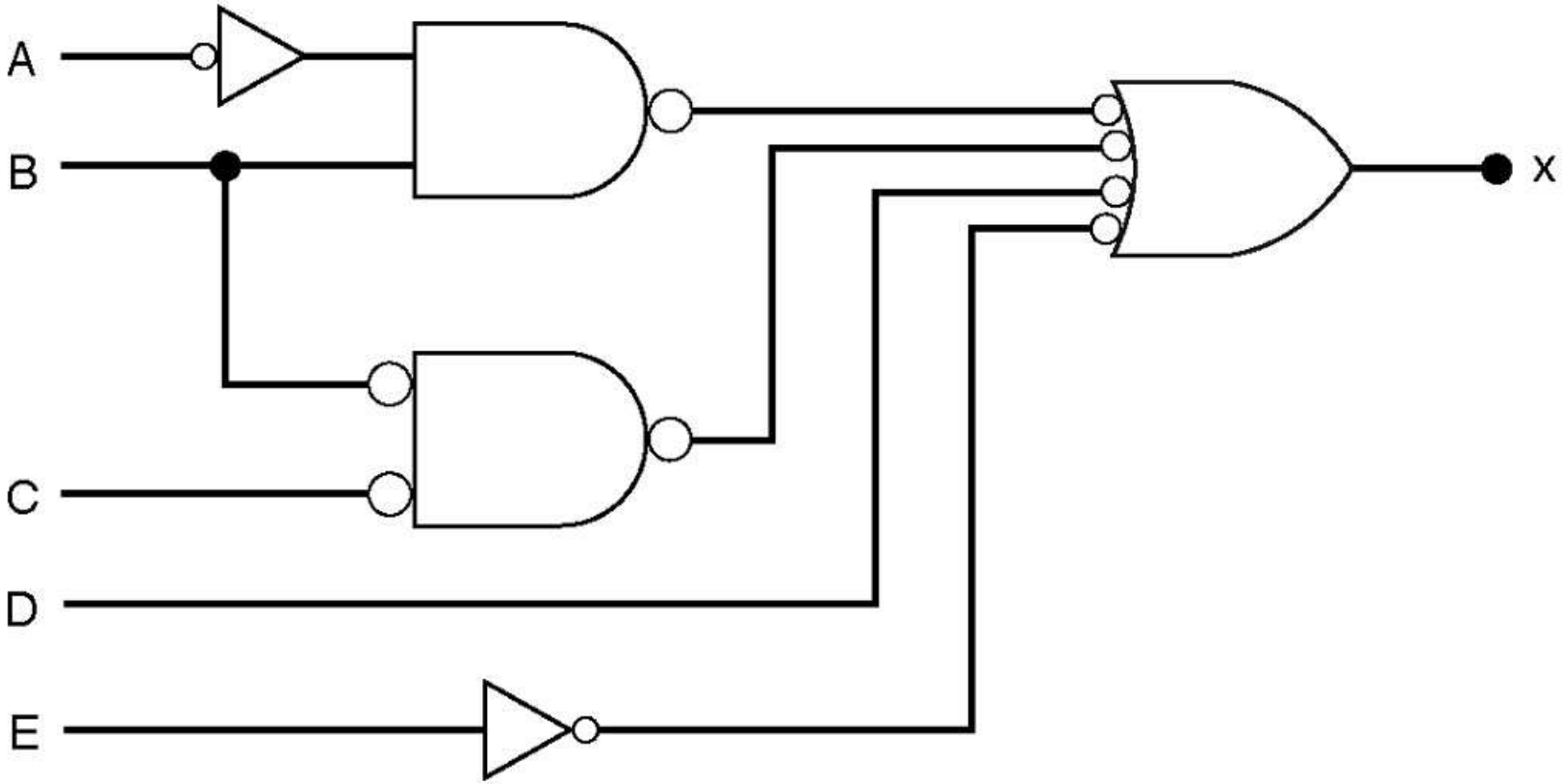


FIGURA 3-48